TOSHIBA

'84

INDUSTRIAL & GENERAL USE

BIPOLAR IC'S

DATA BOOK

TOSHIBA CORPORATION

INTRODUCTION

As observed from the cases of conversion from individual electronic components to microcomputers, recently new electronic components have been rapidly conversed into integrated circuits which have characteristics of high density and low power consumption.

In addition to the conversion, Bipolar IC for general purpose have been widely utilized for not only such industrial machines as telecommunication, measurement equipments, controlling equipments, OA machines but also various consumer appliances such as VTR and audio systems.

In order to satisfy those needs, TOSHIBA has developed and introduced Bipolar IC for general purpose.

This databook contains data sheets of

- Transistor Array / Interface Driver Series
- Operational Amplifier / Voltage Comparator / Timer Series
- Regulator Series

for professional, industrial and consumer applications.

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INDUSTRIAL AND GENERAL USE BIPOLAR IC

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Transistor Array Interface Driver

Series

ALPHANUMERIC INDEX

Transistor Array/Interface Driver

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SELECTION GUIDE

INDEX/SELECTION GUIDE

	TYPE NO.	FUNCTION	UNIT	CLAMP DIODE	V_{OUT} (V)	I_{OUT} (mA)	R_{IN} (Ω)	SYSTEM V_{CC}(V)	OUT-LINE
*	TD62001AP	Darlington Driver	7	○	50	500	None	Free	DIP16
*	TD62002AP	"	"	○	"	"	10.5K +7VZ.D.	14∿25	"
	TD62003AP	"	"	○	"	"	2.7K	5	"
	TD62004AP	"	"	○	"	"	10.5K	6∿15	"
	TD62006P	"	6	○	22	150	20K	6 ∿ 20	DIP14
	TD62007P	"	7	○	"	"	"	"	DIP16
*	TD62064AP	High Current Darlington Driver	4	○	50	1500	230	5	"
*	TD62074AP	Isolated Darlington Driver	"		"	"	"	"	"
*	TD62081AP	Darlington Driver	8	○	"	500	None	Free	DIP18
*	TD62082AP	"	"	○	"	"	10.5K +7VZ.D.	14∿25	"
	TD62083AP	"	"	○	"	"	2.7K	5	"
	TD62084AP	"	"	○	"	"	10.5K	6 ∿ 15	"
	TD62101P	"	7		25	"	None	Free	DIP16
	TD62103P	"	"		"	"	2.7K	5	"
	TD62104P	"	"		"	"	10.5K	6 ∿ 15	"
	TD62105P	"	"		"	"	20K	12∿25	"
	TD62107P	Darlington Driver with Enable	4	○	45	750	LSTTL Compati.	5	"
	TD62301P	Low Saturation Driver	7	○	15	200	2K	"	"
	TD62302P	"	"	○	"	"	8.4K	"	"
	TD62303P	6 Digit Driver	6		"	500	LSTTL Compati.	"	"
*	TD62304AP	Low Input Active Driver	7		50	"	"	"	"
	TD62305AP	"	"		"	"	"	"	"
	TD62306P	Low Saturation Driver	6	○	20	150	20K	5 ∿ 18	DIP14
	TD62307P	"	7	○	"	"	"	"	DIP16
*	TD62308AP	Low Input Active Driver	4	○	50	1500	LSTTL Compati.	5	"
	TD62476P	Dual Peripheral AND Driver	2	○	35	350	"	"	DIP 8
	TD62477P	" NAND "	"	○	"	"	"	"	"
	TD62478P	" OR "	"	○	"	"	"	"	"
	TD62479P	" NOR "	"	○	"	"	"	"	"

INDEX/SELECTION GUIDE (CONTINUED)

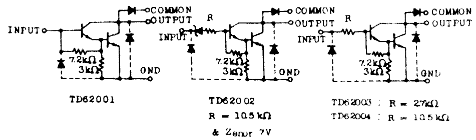
TYPE NO.	FUNCTION	UNIT	CLAMP DIODE	V_{OUT} (V)	I_{OUT} (mA)	R_{IN} (Ω)	SYSTEM V_{CC}(V)	OUT-LINE
TD62501P	Single Driver (Common Emitter)	7		35	200	None	Free	DIP16
TD62502P	" "	"		"	"	10.5K +7VZ.D.	14∿25	"
TD62503P	" "	"		"	"	2.7K	5	"
TD62504P	" "	"		"	"	10.5K	6 ∿ 15	"
TD62505P	Single Driver (Common Collector)	7		35	200	None	Free	"
TD62506P	" "	"		"	"	2.7K	5	"
TD62507P	" (Isolated)	5		"	"	None	Free	"
TD62551S	" (Common Emitter)	4		25	150	"	"	SIP 9
TD62553S	" "	"		"	"	2.7K	5	"
TD62554S	" "	"		"	"	10.5K	6 ∿ 15	"
TD62555S	" "	"		"	"	20K	12∿25	"
TD62601P	6 V_{TH} Free Driver (INV)	6		20	10	1M	4 ∿ 18	DIP16
TD62602P	" (INV, O.C.)	"		"	"	"	"	"
TD62603P	" (NON, INV)	"		"	"	"	"	"
TD62604P	" (NON,INV,O.C)	"		"	"	"	"	"
TD62703P	High Voltage Source Driver	"		60	50	2.7K	5	DIP14
TD62705P	"	"		"	"	57K	6 ∿ 15	DIP16
TD62706P	"	"		"	"	20K	5	"
* TD62781AP	" (with pull-down resistor)	8		"	"	(10K)	"	DIP18
* TD62782AP	" "	"		"	"	(")	6 ∿ 15	"
TD62801P	8 Bit Shift Register/Latch/ Driver	1		26	70	LSTTL Compati.	5	DIP16
TD62803P	Stepping Motor Controller/ Driver	"		28	400	"	"	"

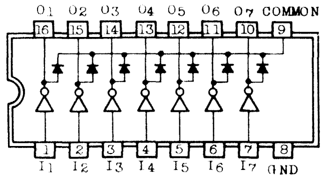
* AP T_{opr}=-40 ∿ +85°C New Product or Under Development

PIN ASSIGNMENTS

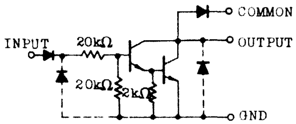
PIN CONNECTIONS AND SCHEMATICS

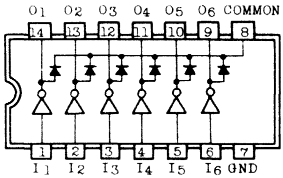
DARLINGTON DRIVER
TD62001AP, TD62002AP, TD62003AP, TD62004AP



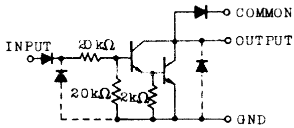


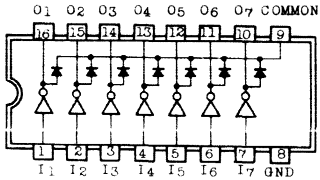
DARLINGTON DRIVER
TD62006P



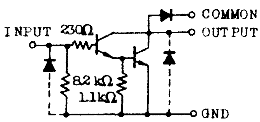


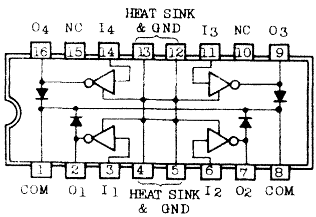
DARLINGTON DRIVER
TD62007P



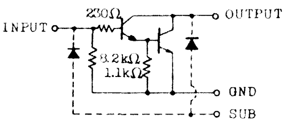


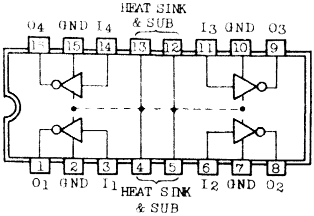
HIGH CURRENT DARLINGTON DRIVER
TD62064AP



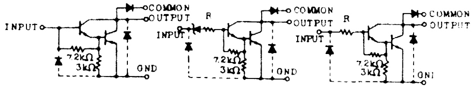


ISOLATED DARLINGTON DRIVER
TD62074AP





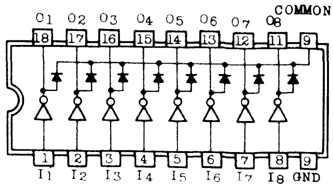
DARLINGTON DRIVER
TD62081AP, TD62082AP, TD62083AP, TD62084AP



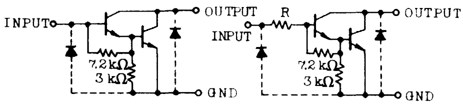
62081

62082
R= 10.5kΩ
& Zener 7V

62083 : R=2.7kΩ
62084 : R=10.5kΩ

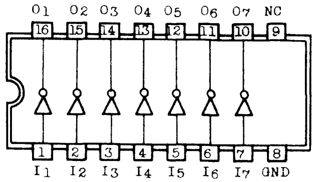


DARLINGTON DRIVER
TD62101P, TD62103P, TD62104P, TD62105P

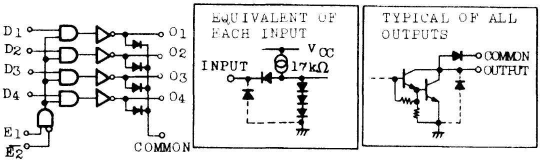


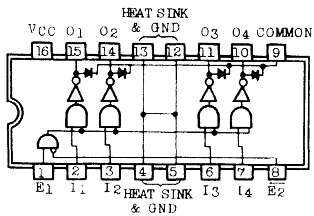
TD62101P

TD62103P: R = 2.7kΩ
TD62104P: R = 10.5kΩ
TD62105P: R = 20.0kΩ

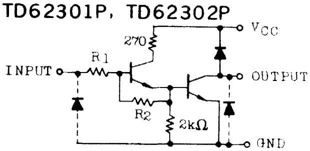


DARLINGTON DRIVER WITH ENABLE
TD62107P



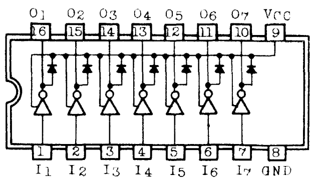


LOW SATURATION DRIVER
TD62301P, TD62302P

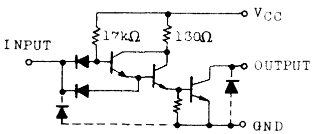


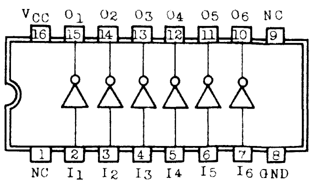
TD62301P
R1 = 2kΩ
R2 = 20kΩ

TD62302P
R1 = 8.4kΩ
R2 = 15kΩ

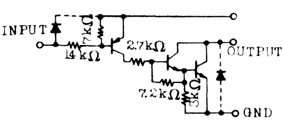


6 DIGIT DRIVER
TD62303P

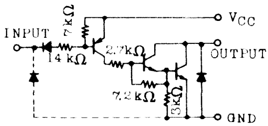




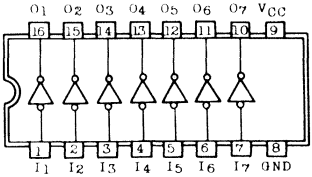
LOW INPUT ACTIVE DARLINGTON DRIVER
TD62304AP, TD62305AP



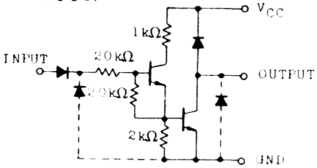
62304

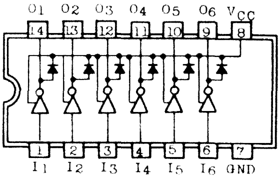


62305

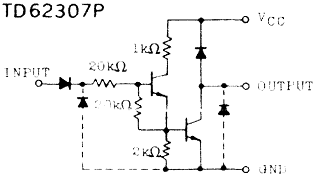


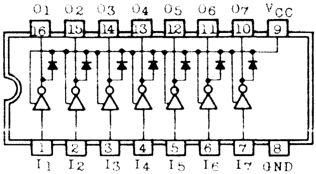
LOW SATURATION DRIVER
TD62306P



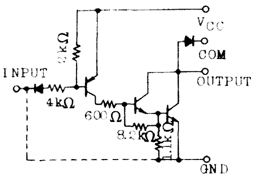


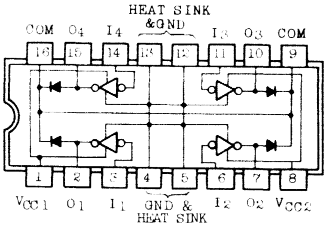
LOW STATURATION DRIVER
TD62307P



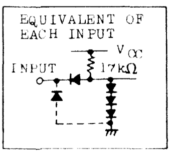


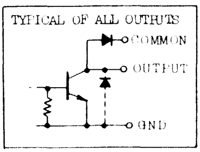
LOW INPUT ACTIVE DARLINGTON DRIVER
TD62308AP

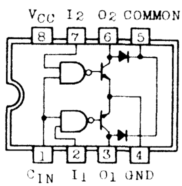




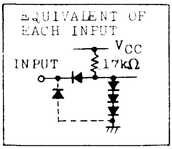
DUAL PERIPHERAL AND DRIVER
TD62476P

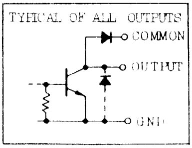


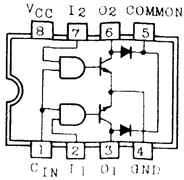




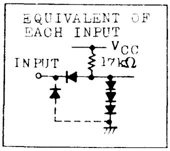
DUAL PERIPHERAL NAND DRIVER
TD62477P

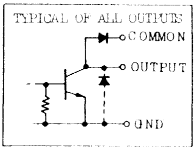


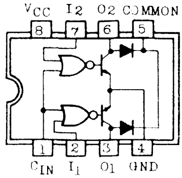




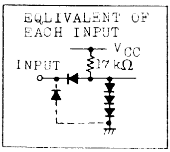
DUAL PERIPHERAL OR DRIVER
TD62478P

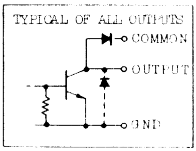


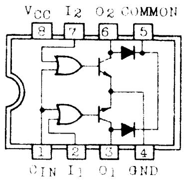




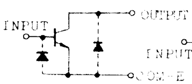
DUAL PERIPHERAL NOR DRIVER
TD62479P



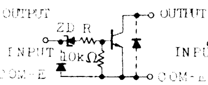




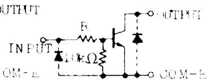
SINGLE DRIVER (COMMON EMITTER)
TD62501P, TD62502P, TD62503P



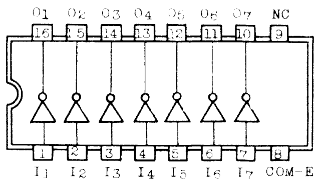
TD62501P



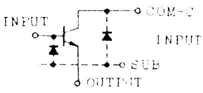
TD62502P R = 10.5 kΩ & Zenor 7V



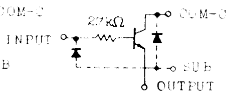
TD62503P R=2.7kΩ
TD62504P R=10.5kΩ



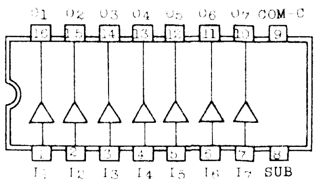
SINGLE DRIVER (COMMON COLLECTOR)
TD62505P, TD62506P



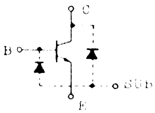
TD62505P

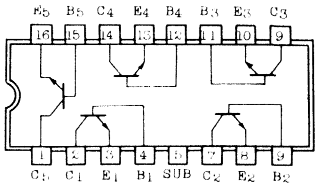


TD62506P

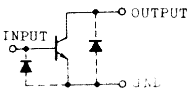


ISOLATED SINGLE TRANSISTOR ARRAY
TD62507P

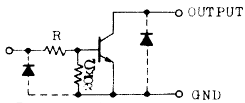




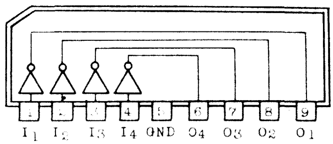
SINGLE DRIVER (COMMON EMITTER)
TD62551S, TD62553S, TD62554S, TD62555S



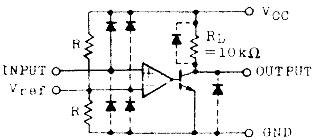
TD62551S



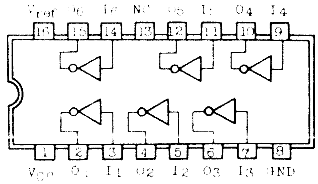
TD62553S : R= 2.7kΩ
TD62554S : R= 10.5kΩ
TD62555S : R= 20kΩ



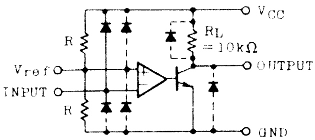
6 THRESHOLD FREE DRIVER
TD62601P, TD62603P (OPEN COLLECTOR)



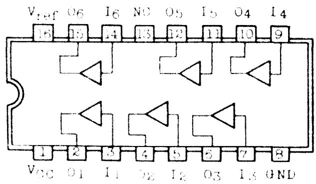
TD62601P: WITH RL
TD62602P: WITHOUT RL



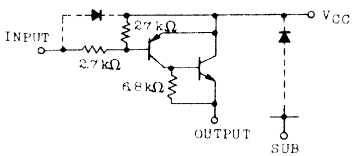
6 THRESHOLD FREE DRIVER
TD62602P, TD62604P (OPEN COLLECTOR)

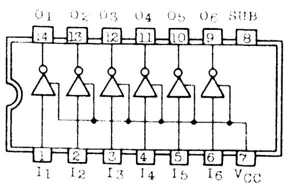


TD62603P: WITH RL
TD62604P: WITHOUT RL

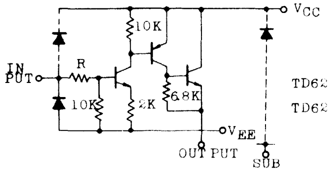


HIGH VOLTAGE SOURCE CURRENT DRIVER
TD62703P

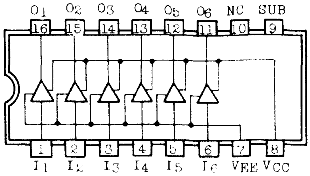




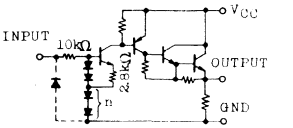
HIGH VOLTAGE SOURCE CURRENT DRIVER
TD62705P, TD62706P



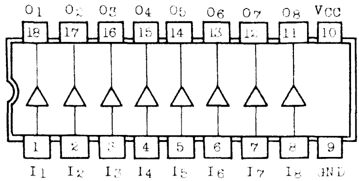
TD62705P: R= 4.7kΩ
TD62706P: R= 10kΩ



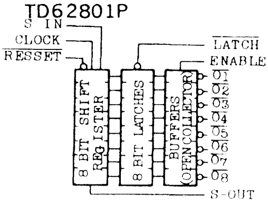
HIGH VOLTAGE SOURCE CURRENT DRIVER
TD62781AP, TD62782AP

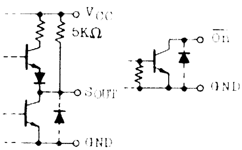


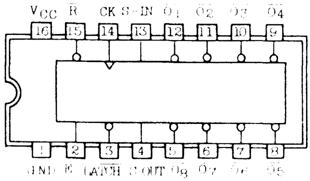
TD62781AP: n=1, TD62782AP: n =4



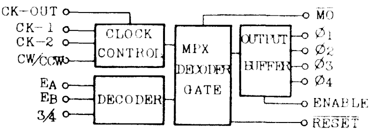
8 BIT SHIFT REGISTER/LATCH/DRIVER
TD62801P

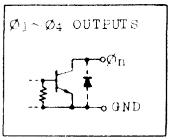


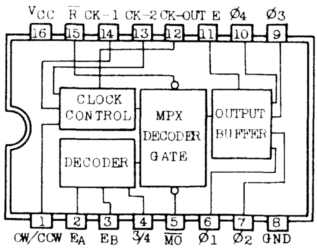




STEPPING MOTOR CONTROLLER/DRIVER
TD62803P







GENERAL

GENERAL

1. Transistor Array/Interface Driver

The Transistor Array/Interface Driver series are suitable for driving such peripheral components as hammers (printers), relays, solenoids, micromotors, and a variety of indicators (LED, fluorscent displays and lamps) and also suitable for many interfaces.
These series are comprised of input current limiting resistors, level-shifting zener diodes, clamp diodes for inductive loads or digital circuits as logic gate, and it is posible to select optimum IC according to use.

2. Basic Circuit of Darlington Transistor

The basic circuit of darlington transistor which is the most representation Transistor Array/Interface Driver is shown in Fig. 1.

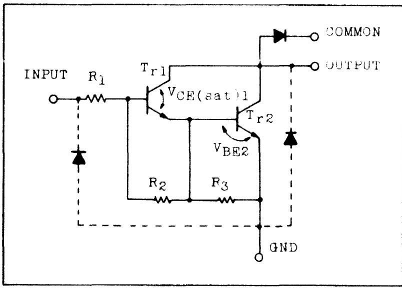


Fig. 1

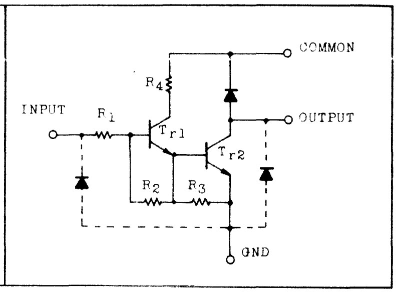


Fig. 2

In darlington circuit, the h_{FE} of transistor is very high. However, its saturation voltage $V_{CE(sat)}$ is the sum of $V_{CE(sat)1}$ (the saturation voltage of the first stage transistor T_{r1}) and V_{BE2} (the base-emitter voltage which is required for the second stage transistor T_{r2} to switch

ON: 0.7V TYP). This voltage is higher than that of a single transistor by V_{BE2}.

$$\boxed{V_{CE(sat)2} = V_{CE(sat)1} + V_{BE2(ON)}}$$

Futher, the diodes shown in dotted line are parasitic diodes which are produced inevitably from the structure of IC.
These diodes will be described later in Section 3 "Chip Structure and Parasitic Elements".

Then, a circuit that is slightly changed from the derlington circuit is shown in Fig. 2.
If the collectors are not used commonly as in this circuit, the saturation voltage of the circuit is lowered to be the same as $V_{CE(sat)2}$ of a single transistor T_{r2}; whereas h_{FE} can be made higher through two-stage amplification, the same as shown in Fig. 1.

Resistor R_1 is a base input current limiting resistor and resistor R_2 and R_3 are provided to bypass leak current to the ground so that transistor T_{r1} and T_{r2} in OFF state can not be switched ON by fine leak current. Futher the bypass made of R_2 and R_3 also serve to discharge the stored charge of the base which is released when T_{r1} and T_{r2} are switched OFF; thus the bypass improves the switching characteristics.

3. Chip Structure and Parasitic Elements

To obtain the high voltage output characteristic for the transistor Array /Interface Driver series, various ideas are incorporated in the design and process such as increased thickness and resistivity of the N doped epitaxial layer. Further, in order to reduce the saturation voltage $V_{CE(sat)}$, the series resistivity of the collector is decreased by N^+ plug, which is driven sufficiently to contact the N^+ buried layer.

The structure of the ship is shown in Fig. 3.

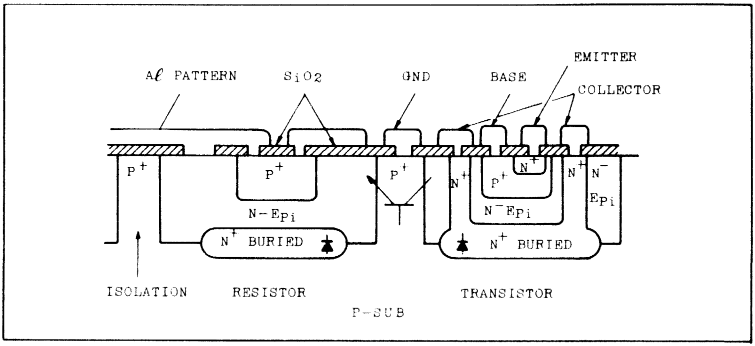


Fig. 3

As for the parasitic elements, there are parasitic diodes which are formed by P-N junction between P-SUB and collector layer of each element, and lateral P-N-P transistors which are based on P^+isolation.

When lower voltage than P-SUB(GND) is applied to the I/O terminal, this terminal acts as an emitter and performs transistor operation using its adjacent circuit element as a collector.

Generally, characteristics of this parasitic transistor such as h_{FE}, gm, etc. are inferior to those of an ordinary transistor; but the parasitic transistor can cause mutual interference between circuits, damage and destruction of devices, and it is therefore necessary to design a circuit without operating the parasitic transistor.

Diodes shown by dotted line in I/O equivalent circuit diagram are also parasitic. These diodes have such characteristics as its forward voltage (V_F) is 0.6V (TYP.) which is somewhat lower than that of common diodes (0.8V TYP.) and its seies resistivity is as high as several 10 ohms (sveral ohms for a common diode).
Since the current capacity of these parasitic diodes is considerably less than that of a common diode (about 10mA), it is necessary to pay attention so that negative voltage must not be applied to the I/O terminals.

For exmaple, the TD62001AP is shown in Fig. 4.
Both of the input and output parasitic diodes connot be used as clamp diodes. If required in the circuit configuration, discrete diodes should be mounted externally.

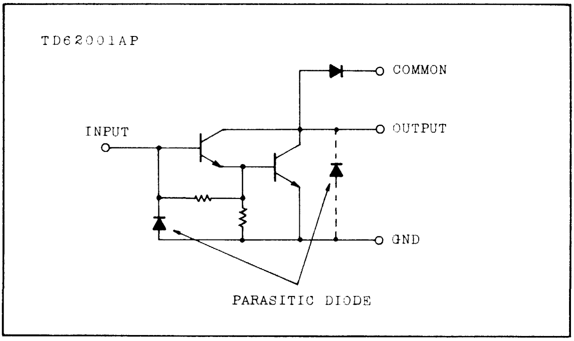


Fig. 4

DESCRIPTION

DESCRIPTION

1. Maximum Ratings

The maximum ratings are the specifications that must not be exceeded to guarantee the life and reliability of ICs. These volues are determined according to the materials, design and manufacturing conditions, and differ from one IC type to another.

Since the maximum ratings refer to absolute maximum ratings, any characteristics among them must never be exceeded during operation even for a monent. If any muximum rating is exceeded, the lost characteristics of IC may not be recovered again.

In designing circuit, therefore, careful concideration should be given to the fluctuation of supply voltage, distribution of the characteristics of electronics parts, ambient temperature changes, input signal variations, etc.; therefore none of the muximum ratings can be exceeded in operation.

2. Recommended Operating Conditions

Following characteristics are generally specified. Therefore, it is recommended to use ICs within these conditions.

(1) Supply Voltage V_{CC}

Supply voltage is specified in the some types of IC which has logic gates at the input stages. Specified value should not be exceeded even under the worst condition of fluctuation of power supply.

(2) Sustaining Voltage $V_{CE(SUS)}$

V_{CEO} is generally specified for collector-emitter breakdown voltage; however, V_{CEO} cannot be measured for this series which have a resistor between the collector and the emitter.
Therefore $V_{CE(SUS)}$ is specified and guaranteed instead of V_{CEO}.
And ICs should be used within the range of this specified sustaining voltage.

(3) Output Current I_{OUT}

I_{OUT} is the allowable volue of current that can be applied when an output transistor is ON.

(4) Input Voltage/Input Current V_{IN}/I_{IN}

V_{IN}/I_{IN} are the allowable volues of voltage/current that can be applied to an input terminal and are indicated in positive or negative values. Hence V_{IN}/I_{IN} in excess of limit is applied, the input circuit may be destroied or disordered functionally.

(5) Clamp Diode Voltage/Current V_R/I_F

V_R/I_F are the allowable values of reverse voltage/forward current for internal clamp diodes used for inductive loads.

(6) Power Dissipation P_D

It is recommended to use this series within the range of maximum junction temperature below 130°C. Therefore, the specified value of power dissipation is that at maximum operating temperature.

3. Electrical Characteristics

(1) Output Leak Current I_{CEX}

This characteristic is tested with the input open-circuited and is the total leak current (collector-to-base, isolation, and substrate). Collector-base leak current is shunted to the common emitter terminal through the base-emitter resistor, and will not be amplified by the darlington input stage.

On the type numbers with logic, "H Level Output Current" I_{OH} is equivalent to this leak current.

(2) Collector-Emitter Saturation Voltage $V_{CE(sat)}$

The saturation voltage of a Darlington circuit is higher than that of a single transistor by $V_{BE(ON)}$ (0.7V TYP.).

The larger the input current is, the better (lower) the saturation voltage becomes. After the input current reaches a certain level, however, its further increase does not affect to the saturation voltage.
On the type numbers with logic, "L Level Output Voltage" V_{OL} is equivalent to this collector-emitter saturation voltage.

(3) DC Current Transfer Ratio h_{FE}
Since a driver having a resistor between the base and the emitter generate a bypass current flow, h_{FE} becomes lower than that of a driver without any bypass flow. Each h_{FE} value takes the bypass current into account.
Hence h_{FE} of a transistor itself is designed to be higher than the h_{FE} specified for practical purpose. Further, this characteristics is not specified for the transistors with three-stage sturucture (Exanple: TD62304AP) or with logic circuit (Example: TD62476P).

(4) Input Current $I_{IN(ON)}$
This test is applied to the type numbers which contain input current limiting elements. Using the Type TD62003AP as an example; the input test voltage (V_{IN}) is set to be the extrapolated maximum for TTL, that is 3.85V.

(5) Input Current $I_{IN(OFF)}$
This characteristic specifies the level of input current which will not produce more than 500μA output leak current at the high temperature limit.
Minimum limit of input current 50μA means that the circuit remains OFF state with output current staying within 500μA so long as the input current will not exceed 50μA.

(6) Input Voltage $V_{IN(ON)}$
Like the Input current test, this characteristic is applied only to those type numbers which contain input current limiting elements.
With the specified maximum input voltage applied, there is a guarantee of at least the level of collector current listed, with a saturation voltage of not more than 2V.

As shown, the maximum Input voltage for each device determines the range of application for that device. Using the Type TD62003AP as an example; the minimum logic "1" output level for standard TTL (2.4V) will result in at least 200mA collector current, the minimum logic "1" output level for low-power shottky TTL (2.7V) will result in at least 250mA collector current, a more realistic logic "1" output level for TTL and most 5V CMOS (3.0V) will result in at least 300mA collector current at an ambient temperature of +25°C.

(7) Clamp Diode Leak Current I_R

This characteristic is the leak current of a clamp diode at reverse bias of the maximum output sustaining voltage.

(8) Clamp Diode Formard Voltage V_F

Each clamp diode is tested for its formard voltage drop at a current level compatible with the maximum output current.

(9) Input Capacitance C_{IN}

This characteristic describes all capacitances associated with each individual input. It is a composite of lead and wire capacitance as well as the junction capacitance.

(10) Turn-ON Delay t_{ON}

This characteristic is measured from the 50% point of the pasitive-going input pulse to the 50% point of the output waveform when switching typical load current.

(11) Trun-OFF Delay t_{OFF}

This characteristic is measured from the 50% point of the negative-going input pulse to the 50% point of the output waveform.

PRECAUTION FOR USE

1. Sustaining Voltage $V_{CE(SUS)}$

Operating inductive loads indicates different characteristics of output voltage and current from those of non-inductive loads as the load is switched OFF.
It is therefore necessary to take sustaining voltage into concideration when a deiver is used at high-voltage and high-current.
If the load line intersects the device output sustaining curve shown in Fig. 5, breakdown occurs at that cross point and secondary breakdown will create device failures.

V_{CEO} is generally specified for collector-emitter breakdown voltage; however, V_{CEO} cannot be measured for this series which have a resistor between the collector and the emitter. Therefore $V_{CE(SUS)}$ is specified and guaranteed instead of V_{CEO}, and ICs should be used within the range of this specified sustaining voltage.

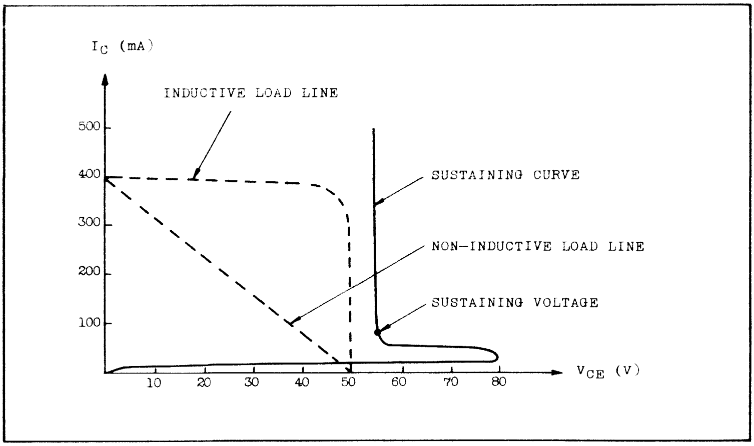


Fig. 5

In the case of inductive loads, high voltage which exceeds $V_{CE(SUS)}$ is generated when the load is switched OFF, but it is posible to absorb such high voltage by a clamp diode.
Using a clamp diode, however, lingthens the switching time which is reeded to cut off the current completely. Therefore to shorten the switching time, a zener diode can be inserted in series with the clamp diode shown in Fig. 6.
In this case it is necessary to select a zener diode under the following condition.

$$\boxed{V_{CC} + V_Z \lessgtr V_{CE(SUS)}}$$

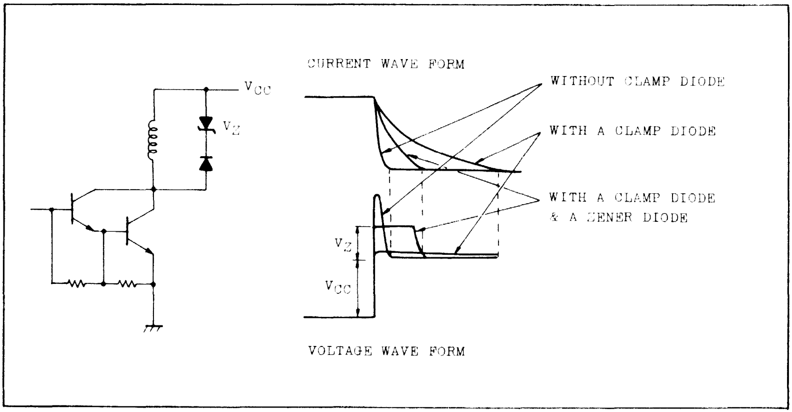


Fig. 6

2. Heat Design

After the sustaining voltage, heat design is probably the very important caution for use.

Even if ICs used within the sustaining voltage, high power operation may increase IC temperatures substantially and are capable of destroying ICs unless appropriate caution are taken.

Therefore, ICs should be used within the recommended operating condition of power dissipation; that is, junction temperature T_j usually is limited to 130°C.

The junction temperature is determined by three parameters (provided that the frequency in use is low).

$$\boxed{T_j = T_A + P_D R_\theta}$$

T_j	: Junction temperature	(°C)
T_A	: Ambient temperature	(°C)
P_D	: Power dissipation	(W)
R_θ	: Thermal resistance	(°C/W)

In the case of TD62001AP series, for example;

$$R_\theta = \frac{150-25}{1.47} = 85 \text{ (°C/W)}$$

when the operating ambient temperature is 50°C;

$$P_D = \frac{130-50}{85} = 0.94 \text{ (W)}$$

The power dissipation P_D is determined by (output current) × (output saturation voltage).

$$\boxed{P_D = n \times I_{OUT} \times V_{CE(sat)}}$$

n	: Number of circuits
I_{OUT}	: Output current
$V_{CE(sat)}$	: Output saturation voltage

If the ON time is less than 0.5 sec, the avarage power dissipation can be calculated from the duty cycle as expressed below.

$$\boxed{P_D = n \times I_{OUT} \times V_{CE(sat)} \times \frac{t_{ON}}{t_{ON}+t_{OFF}}}$$

t_{ON}	: ON time
t_{OFF}	: OFF time

TECHNICAL DATA SHEET

BIPOLAR DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TD62001AP, TD62002AP TD62003AP, TD62004AP

TENTATIVE

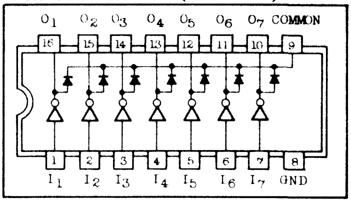
TD62001AP DARLINGTON DRIVER
TD62002AP DARLINGTON DRIVER
TD62003AP DARLINGTON DRIVER
TD62004AP DARLINGTON DRIVER

Features
- Output Current....................500mA Max.
- High Sustaining Voltage Outputs...50V Min.
- Output Clamp Diodes
- Inputs Compatible with Various Types of Logic

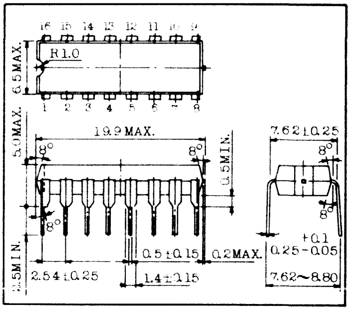
TYPE	INPUT RESISTOR	DESIGNATION
TD62001AP	No (External)	General Purpose
TD62002AP	10.5kΩ+7V Zener Diode	14 ~ 25V P-MOS
TD62003AP	2.7kΩ	TTL, 5V C-MOS
TD62004AP	10.5kΩ	6~15V P-MOS, C-MOS

Description
The TD62001AP Series are high-voltage, high-current darlington arrays comprised of seven NPN darlington pairs.
All units feature integral clamp diodes for switching inductive loads.

PIN CONNECTION (TOP VIEW)



PACKAGE Unit: mm



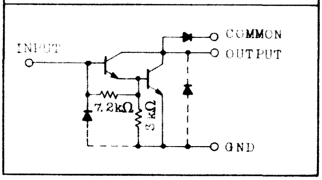
MAXIMUM RATINGS (Ta=25°C unless otherwise noted)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Output Sustaining Voltage		$V_{CE(SUS)}$	50	V
Output Current		I_{OUT}	500	mA
Input Voltage		V_{IN}*	-0.5 ~ +30	V
Input Current		I_{IN}**	25	mA
Clamp Diode	Reverse Voltage	V_R	50	V
	Forward Current	I_F	500	mA
GND Terminal Current		I_{GND}	2.8	A
Power Dissipation		P_D	1.47	W
Operating Temperature		T_{opr}	-40 ~ +85	°C
Storage Temperature		T_{stg}	-55 ~ +150	°C

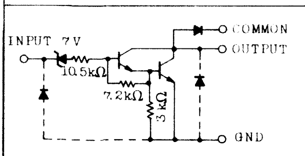
* Except TD62001AP, ** Only TD62001AP

SCHEMATICS (EACH DRIVER)

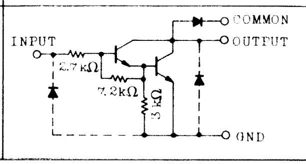
TD62001AP



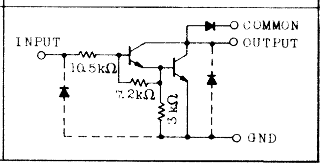
TD62002AP



TD62003AP



TD62004AP



TD62001AP, TD62002AP
TD62003AP, TD62004AP

RECOMMENDED OPERATING CONDITIONS (Ta=-40～+85°C)

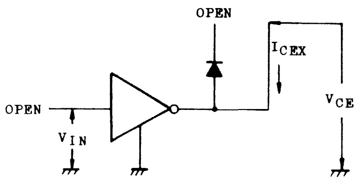
CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Output Sustaining Voltage	$V_{CE(SUS)}$		0		50	V
Output Current	I_{OUT}	T_{PW}=25ms, DF=10%, 7 Circuits	0		400	mA
		T_{PW}=25ms, DF=30%, 7 Circuits	0		200	
Input Voltage	V_{IN}	Except TD62001AP	0		30	V
Input Current	I_{IN}	Only TD62001AP	0		5	mA
Clamp Diode Reverse Voltage	V_R				50	V
Clamp Diode Forward Current	I_F				400	mA
Power Dissipation	P_D				0.52	W

ELECTRICAL CHARACTERISTICS (Ta=25°C unless otherwise noted)

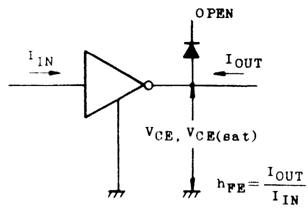
CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Leak Current		I_{CEX}	1	V_{CE}=50V, Ta=25°C			50	μA
				V_{CE}=50V, Ta=85°C			100	
	TD62002AP			V_{CE}=50V, V_{IN}=6V			500	
	TD62004AP			V_{CE}=50V, V_{IN}=1V			500	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$	2	I_{OUT}=350mA, I_{IN}=500μA		1.3	1.6	V
				I_{OUT}=200mA, I_{IN}=350μA		1.1	1.3	
				I_{OUT}=100mA, I_{IN}=250μA		0.9	1.1	
Input Current	TD62002AP	$I_{IN(ON)}$	3	V_{IN}=17V		0.82	1.25	mA
	TD62003AP			V_{IN}=3.85V		0.93	1.35	
	TD62004AP			V_{IN}=5V		0.35	0.5	
				V_{IN}=12V		1.0	1.45	
		$I_{IN(OFF)}$	4	I_{OUT}=500μA, Ta=85°C	50	65		μA
Input Voltage	TD62002AP	$V_{IN(ON)}$	5	V_{CE}=2V, I_{OUT}=300mA			13	V
	TD62003AP			V_{CE}=2V, I_{OUT}=200mA			2.4	
				V_{CE}=2V, I_{OUT}=250mA			2.7	
				V_{CE}=2V, I_{OUT}=300mA			3.0	
	TD62004AP			V_{CE}=2V, I_{OUT}=125mA			5.0	
				V_{CE}=2V, I_{OUT}=200mA			6.0	
				V_{CE}=2V, I_{OUT}=275mA			7.0	
				V_{CE}=2V, I_{OUT}=350mA			8.0	
DC Current Transfer Ratio		h_{FE}	2	V_{CE}=2V, I_{OUT}=350mA	1000			
Clamp Diode Reverse Current		I_R	6	V_R=50V, Ta=25°C			50	μA
				V_R=50V, Ta=85°C			100	
Clamp Diode Forward Voltage		V_F	7	I_F=350mA			2.0	V
Input Capacitance		C_{IN}				15		pF
Turn-ON Delay		t_{ON}	8	V_{OUT}=50V, R_L=163Ω		0.1		μs
Turn-OFF Delay		t_{OFF}		C_L=15pF		0.2		

TEST CIRCUIT

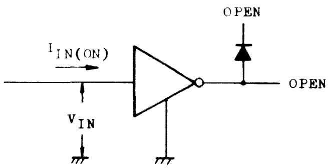
1. I_{CEX}



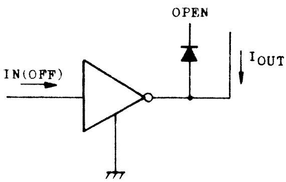
2. $V_{CE(sat)}$, h_{FE}



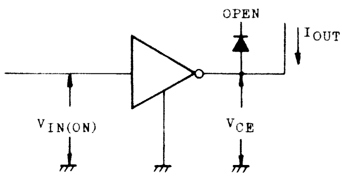
3. $I_{IN(ON)}$



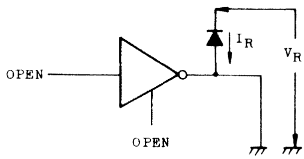
4. $I_{IN(OFF)}$



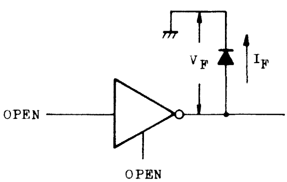
5. $V_{IN(ON)}$



6. I_R

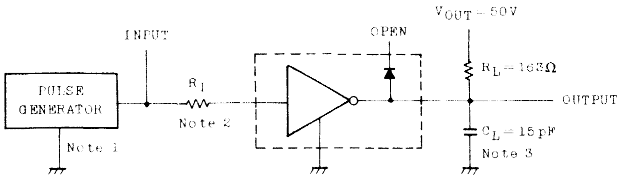


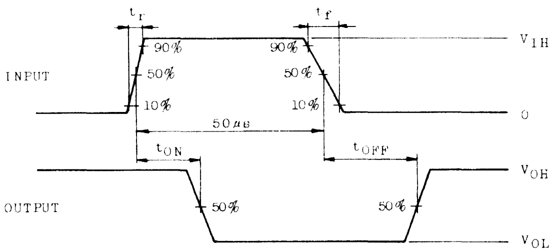
7. V_F



TD62001AP, TD62002AP TD62003AP, TD62004AP

8. t_{ON}, t_{OFF}





Notes: 1. Pulse Width 50μs, Duty Cycle 10%
Output Impedance 50Ω
$t_r \leqq 5ns$, $t_f \leqq 10ns$

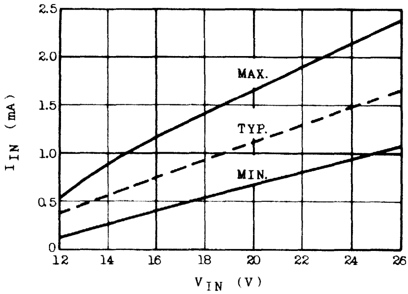
2. See below

Input Conditions

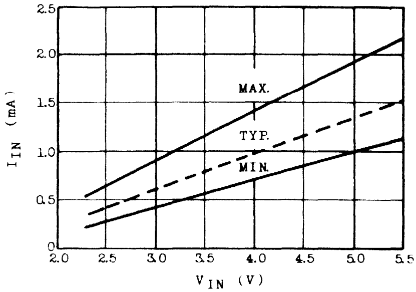
TYPE NUMBER	R_I	V_{IH}
TD62001AP	2.7kΩ	3V
TD62002AP	0	13V
TD62003AP	0	3V
TD62004AP	0	8V

3. C_L includes probe and jig capacitance.

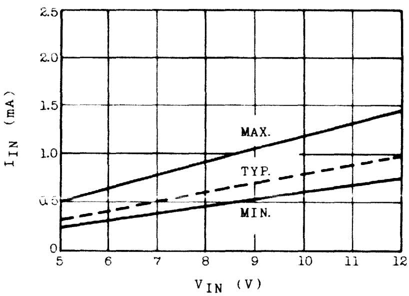
TD62002AP I_{IN} – V_{IN}



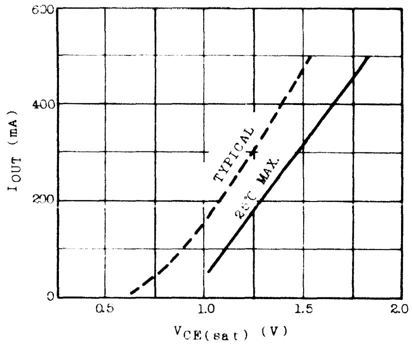
TD62003AP I_{IN} – V_{IN}



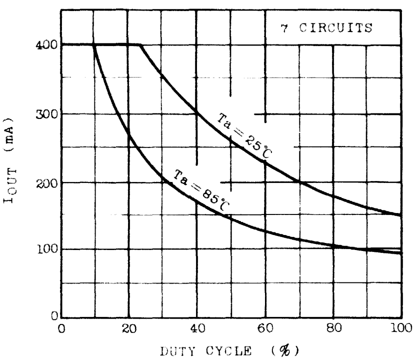
TD62004AP I_{IN} – V_{IN}



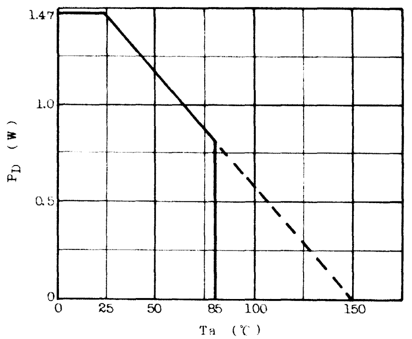
I_{OUT} – $V_{CE(sat)}$



I_{OUT} – DUTY CYCLE



P_D – Ta



TD62006P

BIPOLAR DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TD62006P DARLINGTON DRIVER

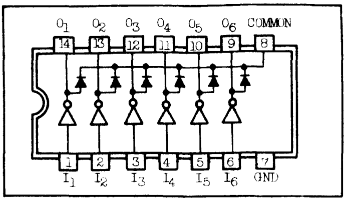
Features

- Output Rating 22V/150mA
- Output Clamp Diodes
- Inputs Compatible with 9∿15V P-MOS, C-MOS.
- Protective Diodes Against a Negative Input Voltage

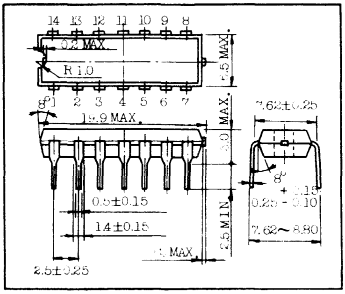
Description

The TD62006P is a high-voltage, high-current darlington array comprised of six NPN darlington pairs.
All units feature integral clamp diodes for switching inductive loads and protective diodes against a negative input voltage.
And the TD62006P is suitable for interfaces from minus and plus dual supply voltage system to plus single supply voltage system.

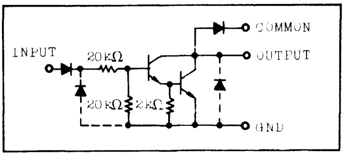
PIN CONNECTION (TOP VIEW)



PACKAGE Unit: mm



SCHEMATICS (EACH DRIVER)



MAXIMUM RATINGS (Ta=25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Output Sustaining Voltage	$V_{CE(SUS)}$	-0.5∿+22	V
Output Current	I_{OUT}	150	mA
Input Voltage	V_{IN}	-37∿+22	V
Clamp Diode Reverse Voltage	V_R clamp	22	V
Clamp Diode Forward Current	I_F clamp	150	mA
GND Terminal Current	I_{GND}	800	mA
Power Dissipation	P_D	1.0	W
Operating Temperature	T_{opr}	-30∿+75	°C
Storage Temperature	T_{stg}	-55∿+150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=-30 ∿ +75°C)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Output Sustaining Voltage	V_{CE}(SUS)		0		20	V
Output Current	I_{OUT}	DC 1 Circuit	0		120	mA
		T_{PW}=25ms, D_F=10%, 6 Circuits	0		100	
Input Voltage	V_{IN}		-35		20	V
Clamp Diode Reverse Voltage	V_R clamp				20	V
Clamp Diode Forward Current	I_F clamp				120	mA
Power Dissipation	P_D				0.44	W

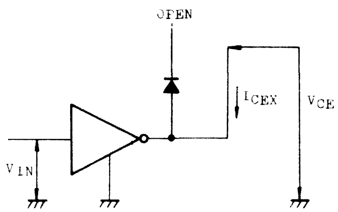
TD62006P

ELECTRICAL CHARACTERISTICS (Ta=25°C)

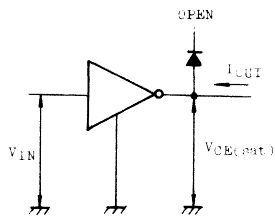
CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Leak Current		I_{CEX}	1	V_{IN}=1.0V, V_{OUT}=20V Ta=75°C			100	μA
Collector-Emitter Saturation Voltage		V_{CE}(sat)	2	V_{IN}=7.5V, I_{OUT}=120mA			1.6	V
DC Forward Current Transfer Ratio		h_{FE}	3	V_{CE}=2.0V, I_{OUT}=120mA	800			
Input Current	Output ON	I_{IN}(ON)	4	V_{IN}=7.5V			0.7	mA
	Output OFF	I_{IN}(OFF)		V_{IN}=-35V			-10	μA
Input Voltage	Output ON	V_{IN}(ON)	5	I_{OUT}=120mA			7.5	V
	Output OFF	V_{IN}(OFF)			1			V
Clamp Diode Leak Current		I_R clamp	6	V_R clamp=20V			30	μA
Clamp Diode Forward Voltage		V_F clamp	7	I_F clamp=120mA			1.6	V
Turn-ON Delay		t_{ON}	8	V_{OUT}=20V, R_L=163Ω C_L=15pF		0.1		μs
Turn-OFF Delay		t_{OFF}				0.4		

TEST CIRCUIT

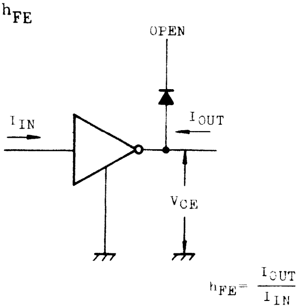
1. I_{CEX}



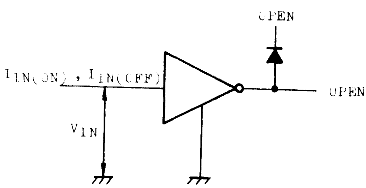
2. V_{CE}(sat)



3. h_{FE}

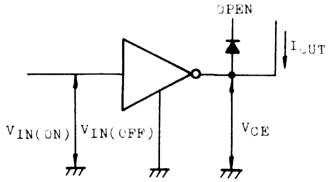


4. I_{IN}(ON), I_{IN}(OFF)

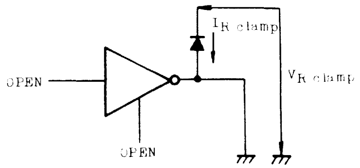


TD62006P

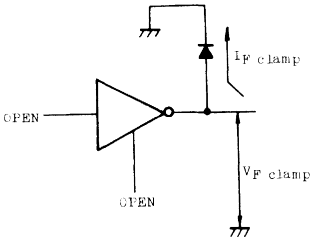
5. $V_{IN}(ON)$, $V_{IN}(OFF)$



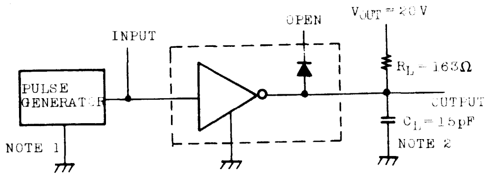
6. I_R clamp

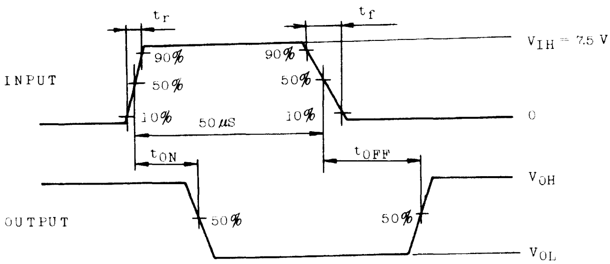


7. V_F clamp



8. t_{ON}, t_{OFF}



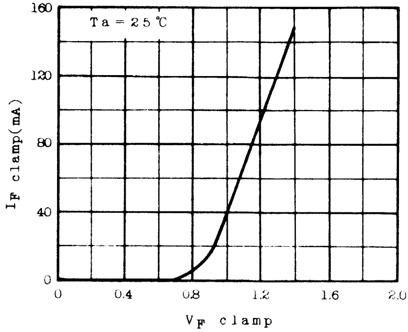


Notes: 1. Pulse Width 50 µS, Duty Cycle 10%
Output Impedance 50Ω
$t_r \leqq 5ns$, $t_f \leqq 10nS$

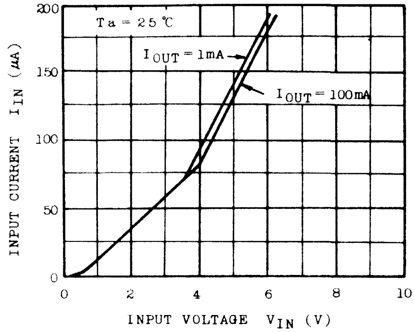
2. C_L includes probe and jig capacitance.

TD62006P

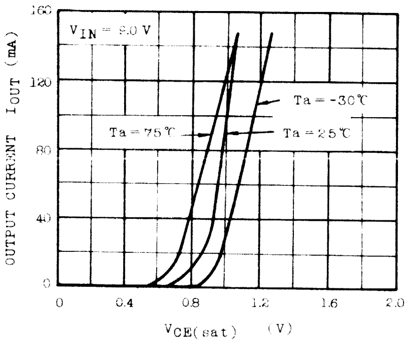
I_F clamp - V_F clamp



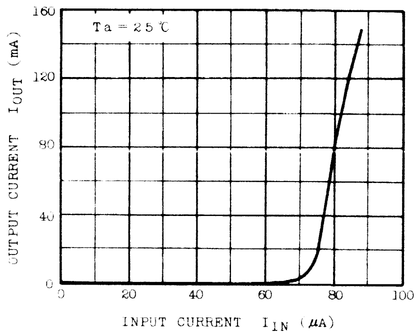
I_{IN} - V_{IN}



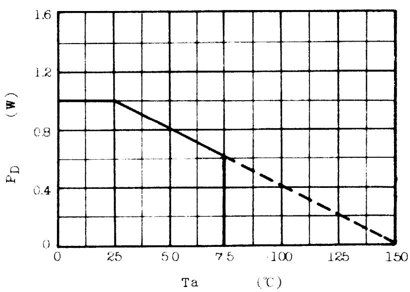
I_{OUT} - V_{CE}(sat)



I_{OUT} - I_{IN}



P_D - Ta



TD62007P

BIPOLAR DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TD62007P DARLINGTON DRIVER

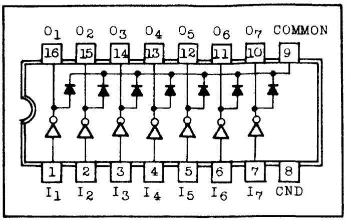
Features

- Output Rating 22V/150mA
- Output Clamp Diodes
- Inputs Compatible with 9 ∿ 15V P-MOS, C-MOS
- Protective Diodes Against a Negative Input Voltage

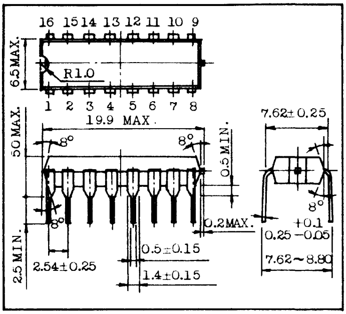
Description

The TD62007P is a high-voltage, high-current darlington array comprised of seven NPN darlington pairs.
All units feature integral clamp diodes for switching inductive loads and protective diodes against a negative input voltage.
And the TD62007P is suitable for interfaces from minus and plus dual supply voltage system to plus single supply voltage system.

PIN CONNECTION (TOP VIEW)



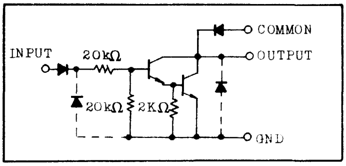
PACKAGE Unit: mm



MAXIMUM RATINGS (Ta=25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Output Sustaining Voltage	$V_{CE(SUS)}$	-0.5 ∿ +22	V
Output Current	I_{OUT}	150	mA
Input Voltage	V_{IN}	-37 ∿ +22	V
Clamp Diode Reverse Voltage	V_R clamp	22	V
Clamp Diode Forward Current	I_F clamp	150	mA
GND Terminal Current	I_{GND}	800	mA
Power Dissipation	P_D	1.0	W
Operating Temperature	T_{opr}	-30 ∿ +75	°C
Storage Temperature	T_{stg}	-55 ∿ +150	°C

SCHEMATICS (EACH DRIVER)



RECOMMENDED OPERATING CONDITIONS (Ta=-30 ∿ +75°C)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Output Sustaining Voltage	$V_{CE(SUS)}$		0		20	V
Output Current	I_{OUT}	DC 1 Circuit	0		120	mA
		T_{PW}=25ms, D_F=10%, 7 Circuits	0		100	
Input Voltage	V_{IN}		-35		20	V
Clamp Diode Reverse Voltage	V_R clamp				20	V
Clamp Diode Forward Current	I_F clamp				120	mA
Power Dissipation	P_D				0.44	W

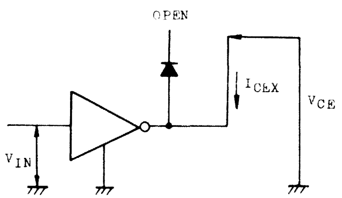
TD62007P

ELECTRICAL CHARACTERISTICS (Ta=25°C)

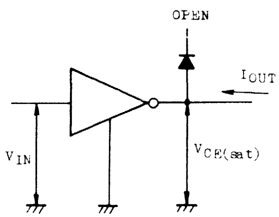
CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Leak Current		I_{CEX}	1	V_{IN}=1.0V, V_{OUT}=20V Ta=75°C			100	μA
Collector - Emitter Saturation Voltage		$V_{CE(sat)}$	2	V_{IN}=7.5V, I_{OUT}=120mA			1.6	V
DC Forward Current Transfer Ratio		h_{FE}	3	V_{CE}=2.0V, I_{OUT}=120mA	800			
Input Current	Output ON	$I_{IN(ON)}$	4	V_{IN}=7.5V			0.7	mA
	Output OFF	$I_{IN(OFF)}$		V_{IN}=-35V			-10	μA
Input Voltage	Output ON	$V_{IN(ON)}$	5	I_{OUT}=120mA			7.5	V
	Output OFF	$V_{IN(OFF)}$			1			V
Clamp Diode Leak Current		I_{R} clamp	6	V_{R} clamp=20V			30	μA
Clamp Diode Forward Voltage		V_{F} clamp	7	I_{F} clamp=120mA			1.6	V
Turn-ON Delay		t_{ON}	8	V_{OUT}=20V, R_L=163Ω C_L=15pF		0.1		μs
Turn-OFF Delay		t_{OFF}				0.4		

TEST CIRCUIT

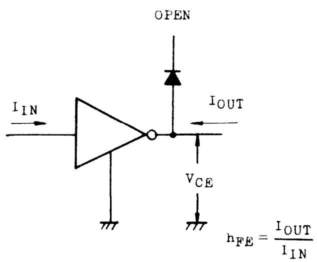
1. I_{CEX}



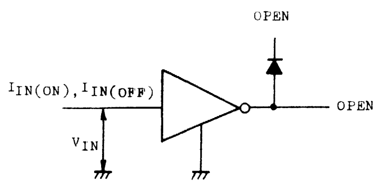
2. $V_{CE(sat)}$



3. h_{FE}

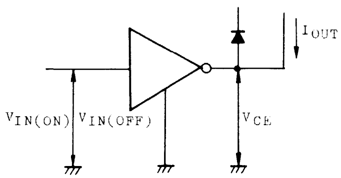


4. $I_{IN(ON)}$, $I_{IN(OFF)}$

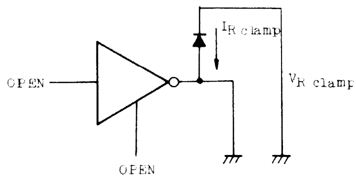


TD62007P

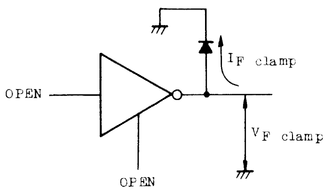
5. $V_{IN(ON)}$, $V_{IN(OFF)}$



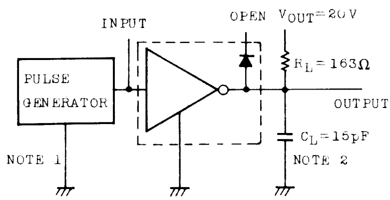
6. I_R clamp

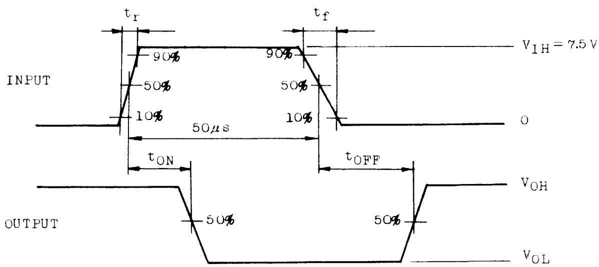


7. V_F clamp



8. t_{ON}, t_{OFF}

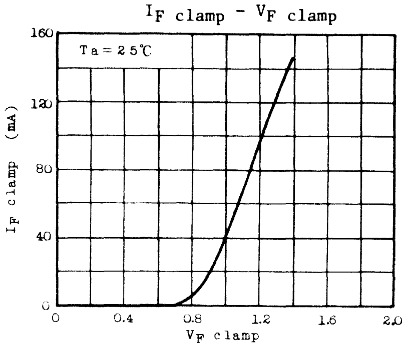


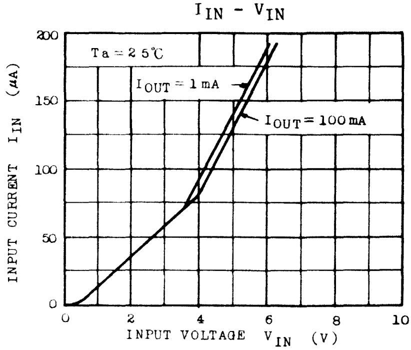


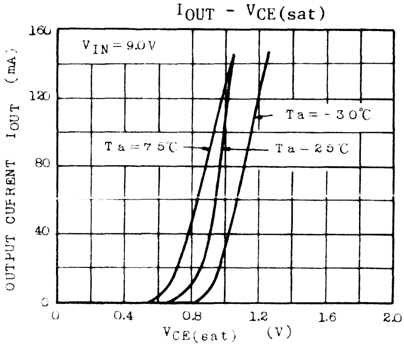
Notes: 1. Pulse Width 50μS, Duty Cycle 10%
Output Impedance 50Ω
$t_r \leq 5nS$, $t_f \leq 10nS$

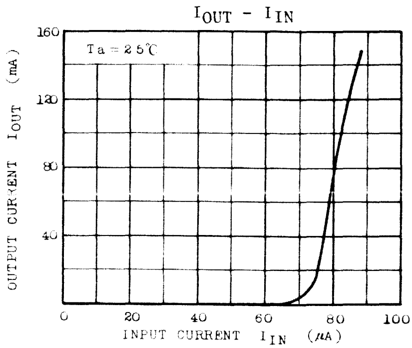
2. C_L includes probe and jig capacitance.

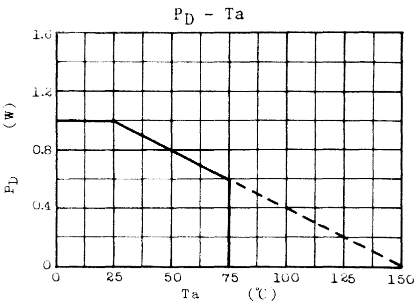
TD62007P


I_F clamp - V_F clamp
Ta = 25℃
I_F clamp (mA)
V_F clamp
0
40
80
120
160
0.4
0.8
1.2
1.6
2.0


I_{IN} - V_{IN}
Ta = 25℃
I_{OUT} = 1 mA
I_{OUT} = 100 mA
INPUT CURRENT I_{IN} (μA)
INPUT VOLTAGE V_{IN} (V)
0
50
100
150
200
2
4
6
8
10


I_{OUT} - $V_{CE(sat)}$
V_{IN} = 9.0 V
Ta = -30℃
Ta = 75℃
Ta = 25℃
OUTPUT CURRENT I_{OUT} (mA)
$V_{CE(sat)}$ (V)
0
40
80
120
160
0.4
0.8
1.2
1.6
2.0


I_{OUT} - I_{IN}
Ta = 25℃
OUTPUT CURRENT I_{OUT} (mA)
INPUT CURRENT I_{IN} (μA)
0
40
80
120
160
20
40
60
80
100


P_D - Ta
P_D (W)
Ta (℃)
0
0.4
0.8
1.2
1.6
25
50
75
100
125
150

TD62064AP, TD62074AP

BIPOLAR DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TENTATIVE

TD62064AP HIGH CURRENT DARLINGTON DRIVER
TD62074AP ISOLATED DARINGTON DRIVER

Features

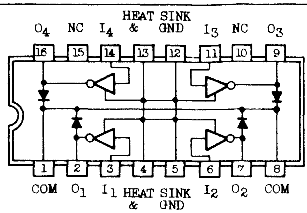
- Output Current....................1.5A Max.
- High Sustaining Voltage 50V
- Input Compatible with TTL and 5V C-MOS
- Output Clamp Diodes...............TD62064AP
- Isolated Darlington Array.........TD62074AP

Description

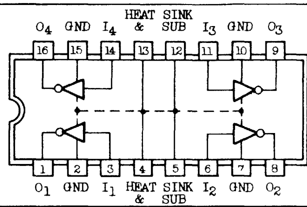
The TD62064AP and TD62074AP are high-voltage, high-current darlington arrays comprised of four NPN darlington pairs.
All units of TD62064AP feature integral clamp diodes for switching inductive loads, and all units of TD62074AP feature uncomitted collectors and emitters for isolated darlington applications.
For proper operation, the substrate (SUB) must be connected to the most negative voltage.

PIN CONNECTIONS (TOP VIEW)

TD62064AP



TD62074AP

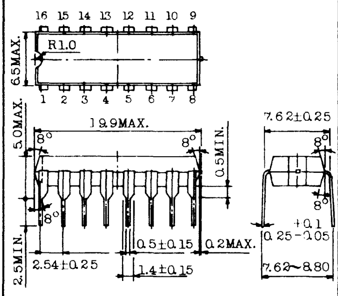


MAXIMUM RATINGS (Ta=25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Output Sustaining Voltage	$V_{CE(SUS)}$	50	V
Output Current	I_{OUT}	1.5	A
Input Current	I_{IN}	50	mA
Input Voltage	V_{IN}	17	V
Clamp Diode Reverse Voltage	V_R *	50	V
Clamp Diode Forward Current	I_F *	1.5	A
Isolation Voltage	V_{SUB} **	50	V
GND Terminal Voltage	I_{GND}	5.0	A
Power Dissipation	P_D	2.7	W
Operating Temperature	Topr	-40 ~ +85	°C
Storage Temperature	Tstg	-55 ~ +150	°C

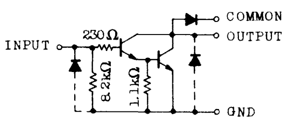
* TD62064AP, ** TD62074AP

PACKAGE Unit: mm

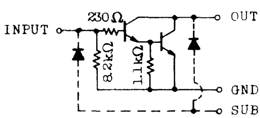


SCHEMATICS (EACH DRIVER)

TD62064AP



TD62074AP



TD62064AP, TD62074AP

RECOMMENDED OPERATING CONDITIONS (Ta=-40~+85°C)

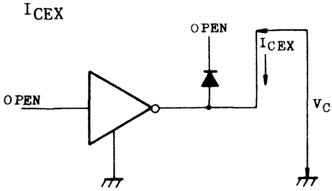
CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Output Sustaining Voltage	$V_{CE(SUS)}$		0		50	V
Output Current	I_{OUT}	T_{PW}=25ms, D_F=8%, 4 Circuits	0		1.25	A
		T_{PW}=25ms, D_F=20%, 4 Circuits	0		0.7	
Input Voltage	V_{IN}		0		8	V
Input Current	I_{IN}		0		20	mA
Clamp Diode Reverse Voltage	V_R				50	V
Clamp Diode Forward Current	I_F				1.25	A
Isolation Voltage	V_{SUB}	TD62074AP			50	V
Power Dissipation	P_D				1.0	W

ELECTRICAL CHARACTERISTICS (Ta=25°C unless otherwise noted)

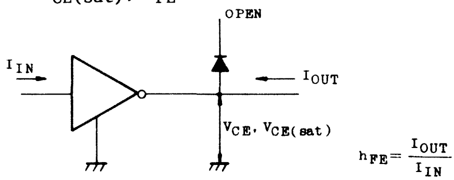
CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Leak Current	I_{CEX}	1	V_{CE}=50V, Ta=25°C			50	μA
			V_{CE}=50V, Ta=85°C			500	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	2	I_{OUT}=1.25A, I_{IN}=2mA			1.6	V
			I_{OUT}=750mA, I_{IN}=935μA			1.25	
DC Forward Current Transfer Ratio	h_{FE}	2	V_{CE}=2V, I_{OUT}=1.25A		1500		
Input Voltag (Output ON)	$V_{IN(ON)}$	3	I_{OUT}=1.25A, I_{IN}=2mA			2.4	V
Clamp Diode Reverse Current	I_R	4	V_R=50V, Ta=25°C			50	μA
			V_R=50V, Ta=85°C			100	
Clamp Diode Forward Voltage	V_F	5	I_F=1.25A			2	V
Input Capacitance	C_{IN}	-			15		pF
Turn-ON Delay	t_{ON}	6	V_{OUT}=50V, R_L=68Ω		0.1		μs
Turn-OFF Delay	t_{OFF}		C_L=15pF		0.2		

TEST CIRCUIT

1. I_{CEX}

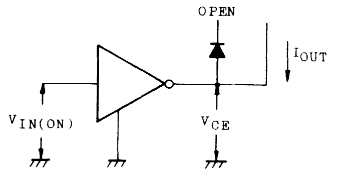


2. $V_{CE(sat)}$, h_{FE}

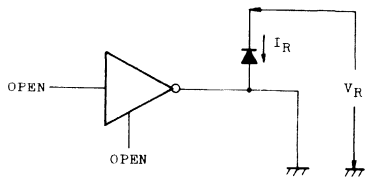


TD62064AP, TD62074AP

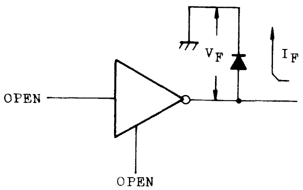
3. $V_{IN(ON)}$



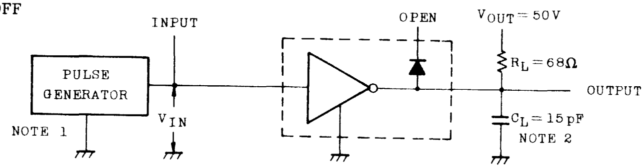
4. I_R

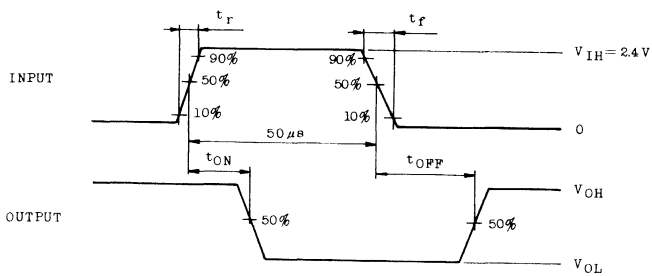


5. V_F



6. t_{ON}, t_{OFF}

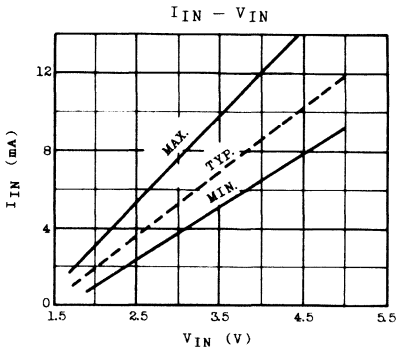


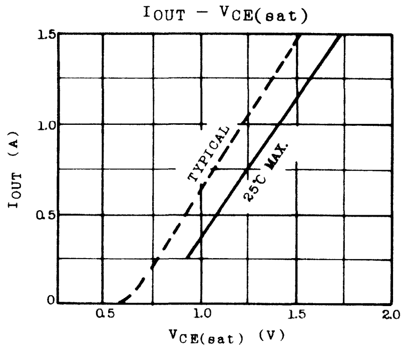


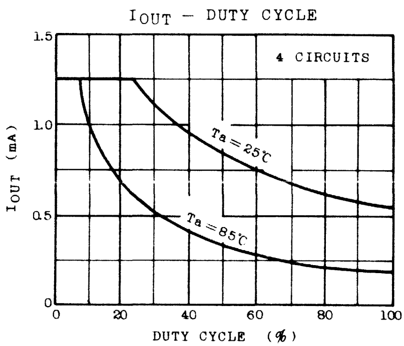
Notes: 1. Pulse Width 50μs, Duty Cycle 10%
Output Impedance 50Ω, $t_r \leq 5$ns, $t_f \leq 10$ns

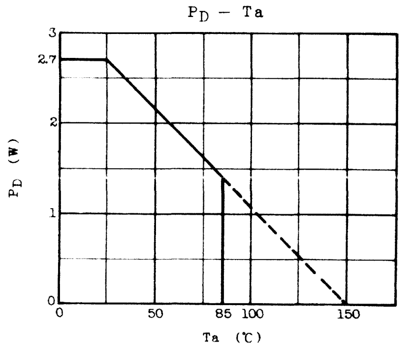
2. C_L includes probe and jig capacitance.

TD62064AP, TD62074AP









TD62081AP, TD62082AP TD62083AP, TD62084AP

BIPOLAR DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TENTATIVE

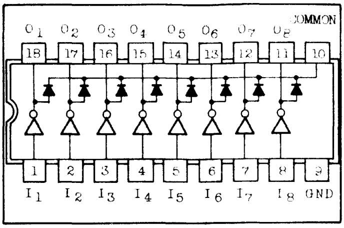
TD62081AP DARLINGTON DRIVER
TD62082AP DARLINGTON DRIVER
TD62083AP DARLINGTON DRIVER
TD62084AP DARLINGTON DRIVER

Features
- Output Current............500mA Max.
- High Sustaining Voltage...50V Min.
- Output Clamp Diode
- Inputs Compatible with Various Types of Logic

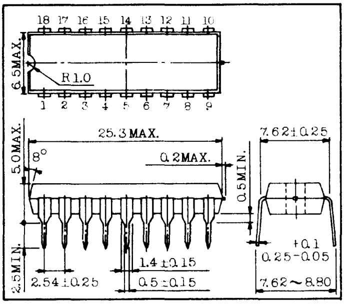
TYPE	INPUT RESISTOR	DESIGNATION
TD62081AP	No (External)	General Purpose
TD62082AP	10.5kΩ+7V Zener Diode	14 ~ 25V P-MOS
TD62083AP	2.7kΩ	TTL, 5V C-MOS
TD62084AP	10.5kΩ	6~15V P-MOS, C-MOS

Description
The TD62081AP Series are high-voltage, high-current darlington arrays comprised of eight NPN darlington pairs.
All units feature integral clamp diodes for switching inductive loads.

PIN CONNECTION (TOP VIEW)



PACKAGE Unit: mm



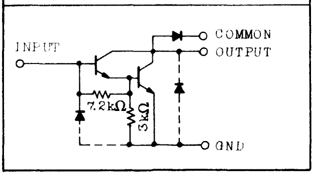
MAXIMUM RATINGS (Ta=25°C unless otherwise noted)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Output Sustaining Voltage		$V_{CE(SUS)}$	50	V
Output Current		I_{OUT}	500	mA
Input Voltage		V_{IN}*	-0.5~ +30	V
Input Current		I_{IN}**	25	mA
Clamp Diode	Reverse Voltage	V_R	50	V
	Forward Current	I_F	500	mA
GND Terminal Current		I_{GND}	3.2	A
Power Dissipation		P_D	1.47	W
Operating Temperature		T_{opr}	-40~ +85	°C
Storage Temperature		T_{stg}	-55~ +150	°C

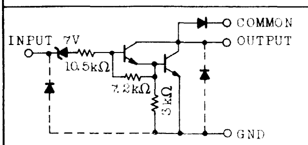
* Except TD62081AP, ** Only TD62081AP

SCHEMATICS (EACH DRIVER)

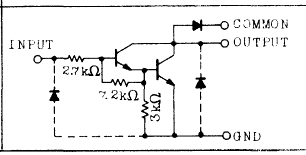
TD62081AP



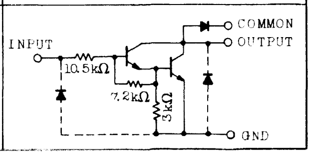
TD62082AP



TD62083AP



TD62084AP



TD62081AP, TD62082AP
TD62083AP, TD62084AP

RECOMMENDED OPERATING CONDITIONS (Ta=−40~ +85°C)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Output Sustaining Voltage	$V_{CE(SUS)}$		0		50	V
Output Current	I_{OUT}	T_{PW}=25ms, DF=8%, 8 Circuits	0		400	mA
		T_{PW}=25ms, DF=25%, 8 Circuits	0		200	
Input Voltage	V_{IN}	Except TD62081AP	0		30	V
Input Current	I_{IN}	Only TD62081AP	0		5	mA
Clamp Diode Reverse Voltage	V_R				50	V
Clamp Diode Forward Current	I_F				400	mA
Power Dissipation	P_D				0.52	W

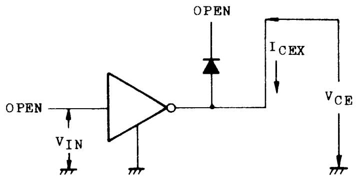
ELECTRICAL CHARACTERISTICS (Ta=25°C unless otherwise noted)

CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Leak Current		I_{CEX}	1	V_{CE}=50V, Ta=25°C			50	μA
				V_{CE}=50V, Ta=85°C			100	
	TD62082AP			V_{CE}=50V, V_{IN}=6V			500	
	TD62084AP			V_{CE}=50V, V_{IN}=1V			500	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$	2	I_{OUT}=350mA, I_{IN}=500μA		1.3	1.6	V
				I_{OUT}=200mA, I_{IN}=350μA		1.1	1.3	
				I_{OUT}=100mA, I_{IN}=250μA		0.9	1.1	
Input Current	TD62082AP	$I_{IN(ON)}$	3	V_{IN}=17V		0.82	1.25	mA
	TD62083AP			V_{IN}=3.85V		0.93	1.35	
	TD62084AP			V_{IN}=5V		0.35	0.5	
				V_{IN}=12V		1.0	1.45	
		$I_{ON(OFF)}$	4	I_{OUT}=500μA, Ta=85°C	50	65		μA
Input Voltage	TD62082AP	$V_{IN(ON)}$	5	V_{CE}=2V, I_{OUT}=300mA			13	V
	TD62083AP			V_{CE}=2V, I_{OUT}=200mA			2.4	
				V_{CE}=2V, I_{OUT}=250mA			2.7	
				V_{CE}=2V, I_{OUT}=300mA			3.0	
	TD62084AP			V_{CE}=2V, I_{OUT}=125mA			5.0	
				V_{CE}=2V, I_{OUT}=200mA			6.0	
				V_{CE}=2V, I_{OUT}=275mA			7.0	
				V_{CE}=2V, I_{OUT}=350mA			8.0	
DC Current Transfer Ratio		h_{FE}	2	V_{CE}=2V, I_{OUT}=350mA	1000			
Clamp Diode Reverse Current		I_R	6	V_R=50V, Ta=25°C			50	μA
				V_R=50V, Ta=85°C			100	
Clamp Diode Forward Voltage		V_F	7	I_F=350mA			2.0	V
Input Capacitance		C_{IN}				15		pF
Turn-ON Delay		t_{ON}	8	V_{OUT}=50V, R_L=163Ω, C_L=15pF		0.1		μs
Turn-OFF Delay		t_{OFF}				0.2		

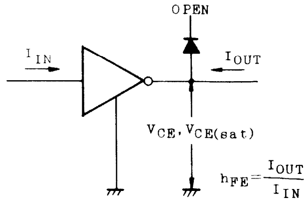
TD62081AP, TD62082AP
TD62083AP, TD62084AP

TEST CIRCUIT

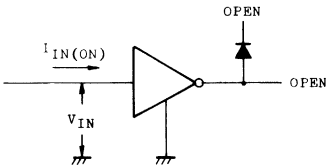
1. I_{CEX}



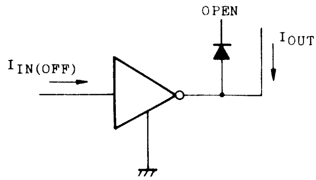
2. $V_{CE(sat)}$, h_{FE}



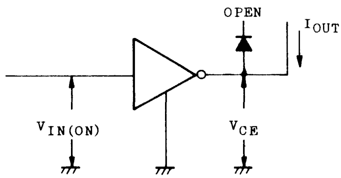
3. $I_{IN(ON)}$



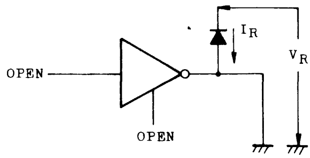
4. $I_{IN(OFF)}$



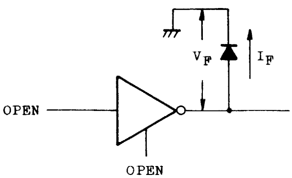
5. $V_{IN(ON)}$



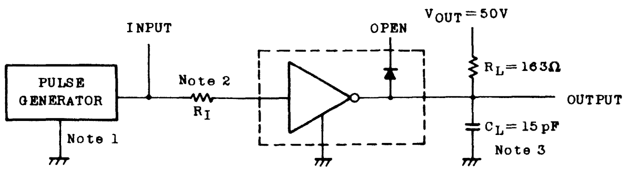
6. I_R

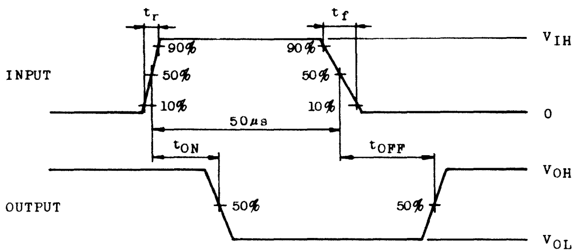


7. V_F



8. t_{ON}, t_{OFF}





Notes: 1. Pulse Width 50μs, Duty Cycle 10%
Output Impedance 50Ω
$t_r \leqq 5$ns, $t_f \leqq 10$ns

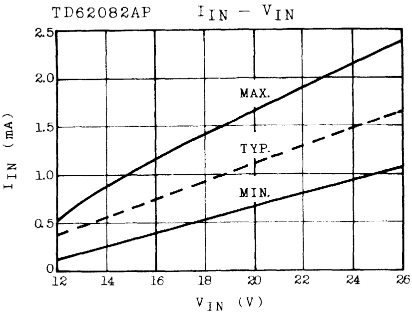
2. See below

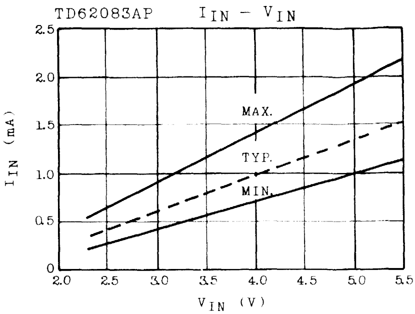
Input Conditions

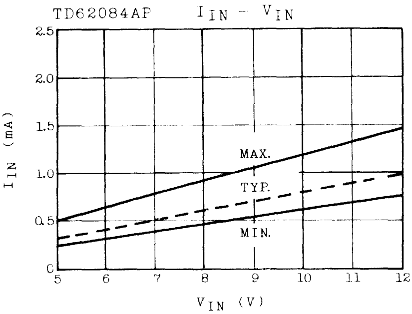
TYPE NUMBER	R_I	V_{IH}
TD62081AP	2.7kΩ	3V
TD62082AP	0	13V
TD62083AP	0	3V
TD62084AP	0	8V

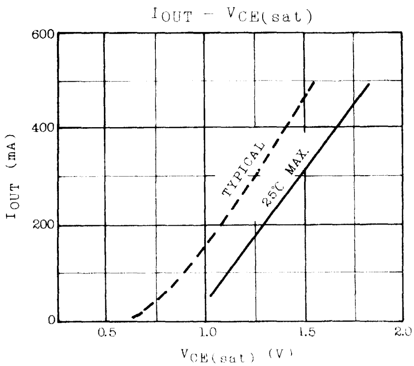
3. C_L includes probe and jig capacitance.

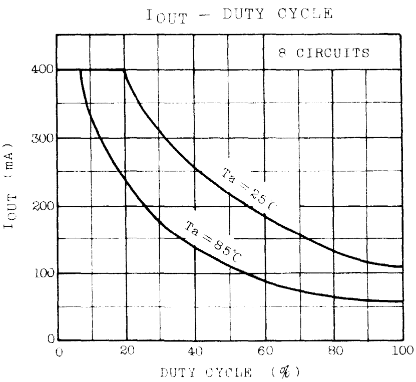
TD62081AP, TD62082AP TD62083AP, TD62084AP

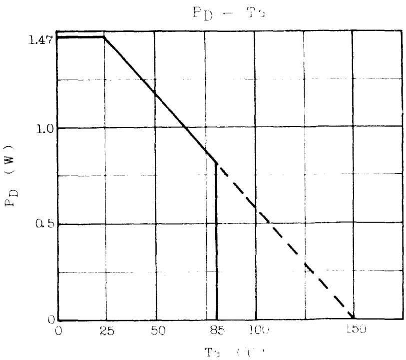












BIPOLAR DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TD62101P, TD62103P
TD62104P, TD62105P

TD62101P DARLINGTON DRIVER
TD62103P DARLINGTON DRIVER
TD62104P DARLINGTON DRIVER
TD62105P DARLINGTON DRIVER

Features

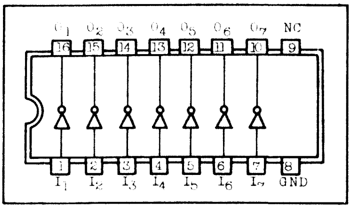
- Output Current .... 500mA Max.
- High Sustaining Voltage Outputs 25V
- Input Compatible with Various Types of Logic

TD62101P Using-external resistor..General Purpose
TD62103P R_{IN}=2.7 kΩ .... TTL, 5V C-MOS
TD62104P R_{IN}=10.5kΩ .... 6∿15V C-MOS, P-MOS
TD62105P R_{IN}=20kΩ .... 12∿25V C-MOS, P-MOS

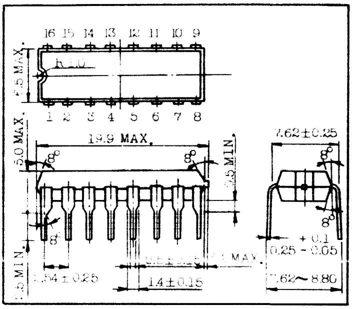
Description

The TD62101P Series are high-voltage, high-current darlington arrays comprised of seven NPN darlington pairs.

PIN CONNECTION (TOP VIEW)



PACKAGE Unit: mm



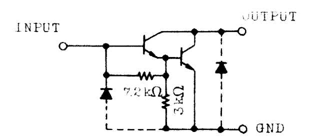
MAXIMUM RATINGS (Ta=25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Output Sustaining Voltage	V_{CE}(SUS)	-0.5 ∿ +25	V
Output Current	I_{OUT}	500	mA
Input Voltage	V_{IN} *	-0.5 ∿ 30	V
Input Current	I_{IN} **	25	mA
GND Terminal Current	I_{GND}	2.3	A
Power Dissipation	P_D	1.0	W
Operation Temperature	T_{opr}	-30 ∿ +75	°C
Storage Temperature	T_{stg}	-55 ∿ +150	°C

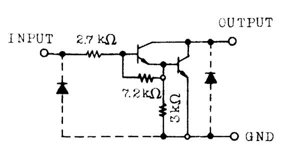
* Except TD62101P, ** Only TD62101P

SCHMATICS (EACH DRIVER)

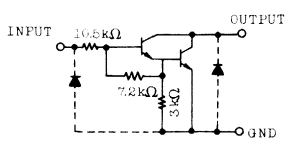
TD62101P



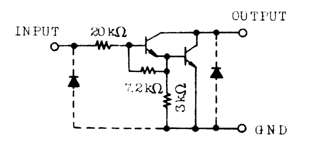
TD62103P



TD62104P



TD62105P



TD62101P, TD62103P
TD62104P, TD62105P

RECOMMENDED OPERATING CONDITIONS (Ta=-30∿+75°C)

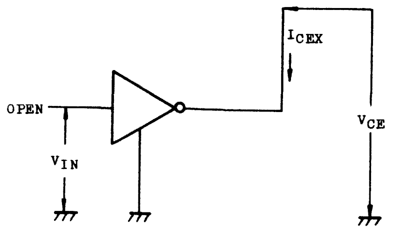
CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Output Sustaining Voltage	V_{CE}(SUS)		0		25	V
Output Current	I_{OUT}	DC 1 Circuit			350	mA
		T_{PW}=25mS, D_F=10%, 7 Circuits			300	mA
Input Voltage	V_{IN}	Except TD62101P			20	V
Input Current	I_{IN}	Only TD62101P			10	mA
Power Dissipation	P_D				0.44	W

ELECTRICAL CHARACTERISTICS (Ta=25°C)

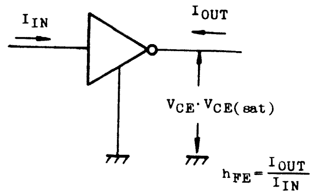
CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Leak Current		I_{CEX}	1	V_{CE}=25V, Ta=75°C, I_{IN}=0			100	μA
Collector-Emitter Saturation Voltage		V_{CE}(sat)	2	I_{OUT}=350mA, I_{IN}=600μA		1.3	2.2	V
				I_{OUT}=200mA, I_{IN}=400μA		1.1	2.0	
				I_{OUT}=100mA, I_{IN}=200μA		1.0	1.8	
DC Forward Current Transfer Ratio		h_{FE}	2	V_{CE}=2V, I_{OUT}=350mA	1000			
Input Current (Output ON)	TD62101P	I_{IN}(ON)	3	V_{IN}=1.5V, I_{OUT}=350mA		0.25		mA
				V_{IN}=1.75V, I_{OUT}=350mA		1.00		
	TD62103P			V_{IN}=2.4V, I_{OUT}=350mA		0.4	0.7	
	TD62104P			V_{IN}=13.5V, I_{OUT}=350mA		1.2	1.7	
	TD62105P			V_{IN}=20.0V, I_{OUT}=350mA		1.0	1.5	
Input Current (Output OFF)		I_{IN}(OFF)	4	I_{OUT}=500μA, Ta=75°C	50	65		μA
Input Voltage (Output ON)	TD62103P	V_{IN}(ON)	5	V_{CE}=2V, I_{OUT}=125mA			2.1	V
	TD62104P						4	
	TD62105P						6.4	
	TD62103P			V_{CE}=2V, I_{OUT}=250mA			2.7	
	TD62104P						7	
	TD62105P						12	
	TD62103P			V_{CE}=2V, I_{OUT}=350mA			3.3	
	TD62104P						8.8	
	TD62105P						15	
Turn-ON Delay		t_{ON}	7	V_{OUT}=25V, R_L=70Ω		0.1		μS
Turn-OFF Delay		t_{OFF}		C_L=15pF,		0.2		

TEST CIRCUIT

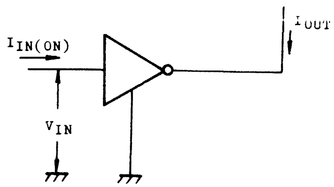
1. I_{CEX}



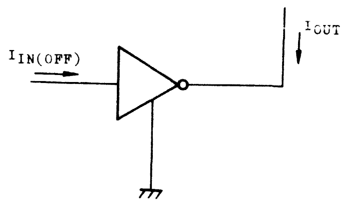
2. h_{FE}, $V_{CE(sat)}$



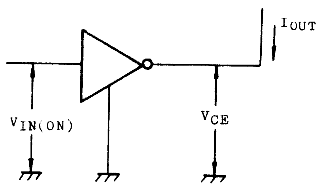
3. I_{IN}(ON)



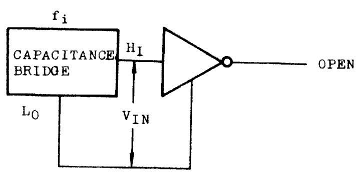
4. I_{IN}(OFF)



5. V_{IN}(ON)

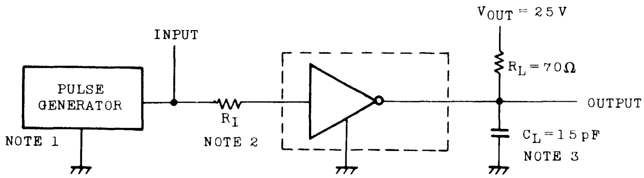


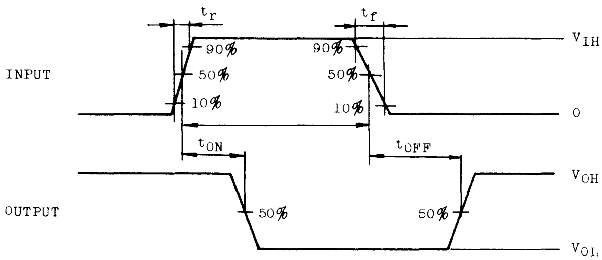
6. C_{IN}



TD62101P, TD62103P
TD62104P, TD62105P

7. t_{ON}, t_{OFF}





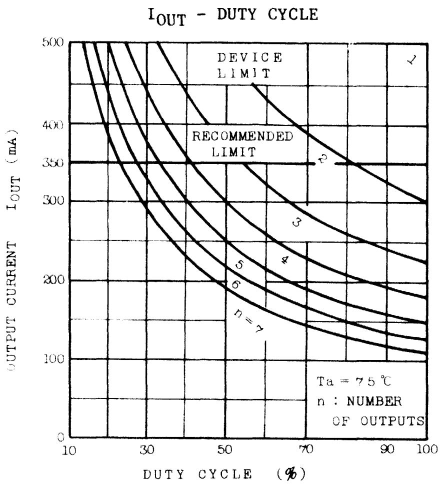
Notes: 1. Pulse Width 50μS, Delay Cycle 10%
Output Impedance 50Ω, $t_r \leqq 5nS$, $t_f \leqq 10nS$

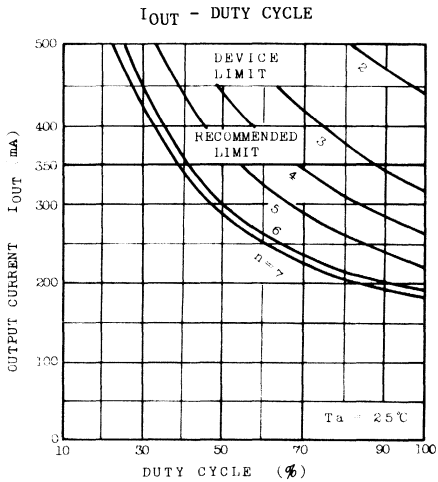
2. See below

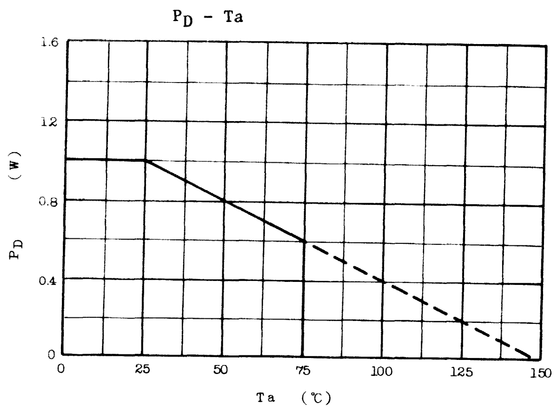
Input Conditions

Type Number	R_I	V_{IH}
TD62101P	2.7kΩ	3 V
TD62103P	0	3 V
TD62104P	0	8 V
TD62105P	0	15 V

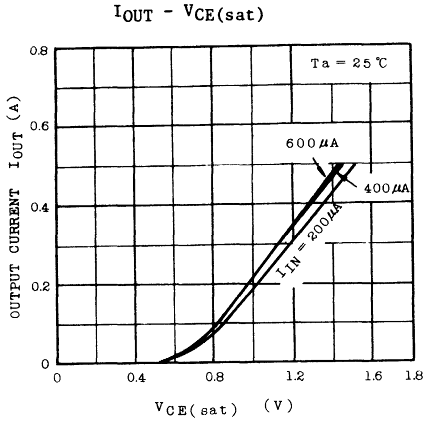
3. C_L includes probe and jig capacitance.

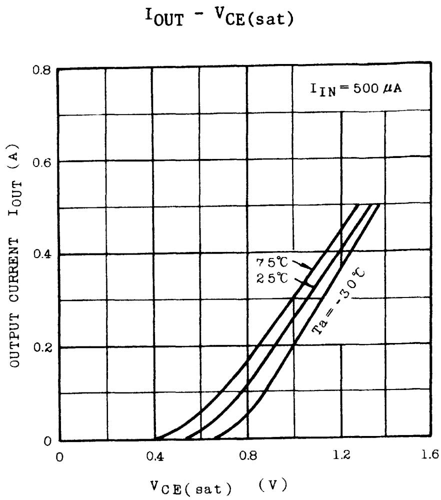

IOUT - DUTY CYCLE
500
400
350
300
200
100
0
10
30
50
70
90
100
OUTPUT CURRENT IOUT (mA)
DUTY CYCLE (%)
DEVICE LIMIT
RECOMMENDED LIMIT
1
2
3
4
5
6
n = 7
Ta = 75 ℃
n : NUMBER OF OUTPUTS

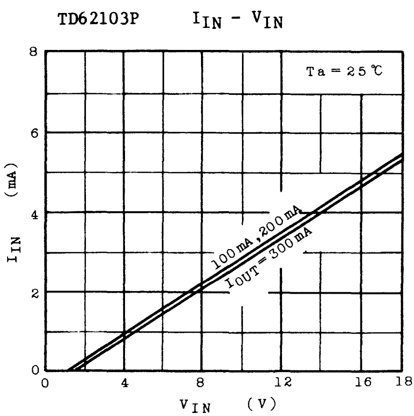

IOUT - DUTY CYCLE
500
400
350
300
200
100
0
10
30
50
70
90
100
OUTPUT CURRENT IOUT (mA)
DUTY CYCLE (%)
DEVICE LIMIT
RECOMMENDED LIMIT
2
3
4
5
6
n = 7
Ta = 25℃

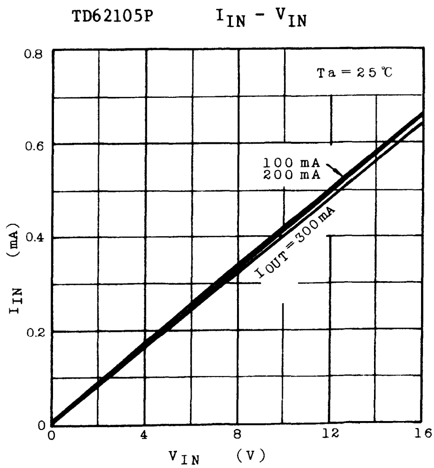

PD - Ta
1.6
1.2
0.8
0.4
0
PD (W)
0
25
50
75
100
125
150
Ta (℃)

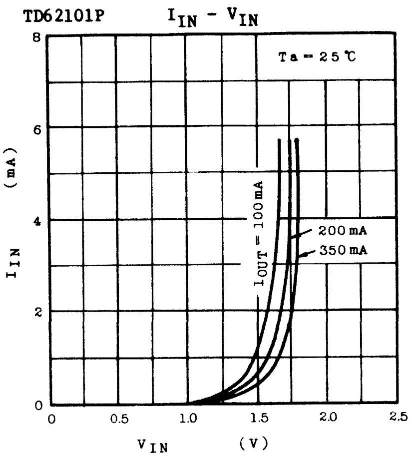
TD62101P, TD62103P
TD62104P, TD62105P

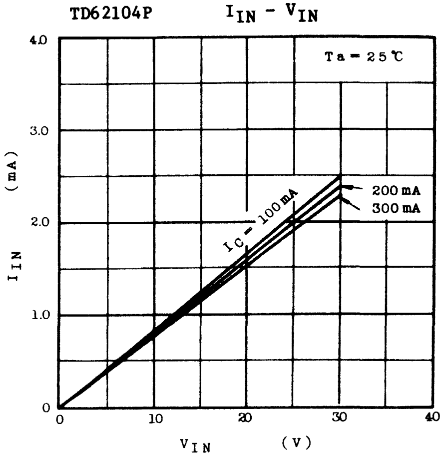


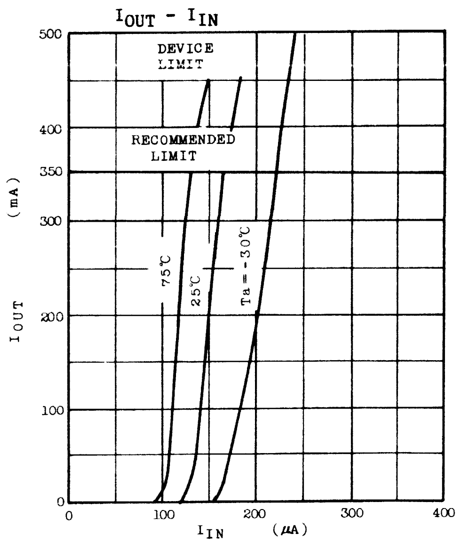







TD62101P
I_{IN} - V_{IN}
Ta = 25℃
I_{OUT} = 100 mA
200 mA
350 mA
I_{IN} (mA)
V_{IN} (V)
0
2
4
6
8
0.5
1.0
1.5
2.0
2.5


TD62104P
I_{IN} - V_{IN}
Ta = 25℃
I_C = 100 mA
200 mA
300 mA
I_{IN} (mA)
V_{IN} (V)
0
1.0
2.0
3.0
4.0
10
20
30
40


I_{OUT} - I_{IN}
DEVICE LIMIT
RECOMMENDED LIMIT
75℃
25℃
Ta = -30℃
I_{OUT} (mA)
I_{IN} (μA)
0
100
200
300
350
400
500
100
200
300
400

TD62107P

BIPOLAR DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TD62107P DARLINGTON DRIVER WITH ENABLE

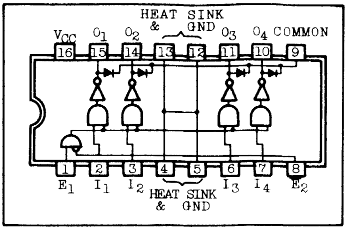
Features

- Output Current .... 750mA Max.
- High Sustaining Voltage Outputs 45V
- Output clamp Diodes
- Enable Inputs .... E_1, $\overline{E_2}$
- Inputs Compatible with TTL and 5V C-MOS
- Wide Supply Voltage Range ... V_{CC}=4.75 ∿ 17V
- GND Terminal=HEAT SINK

Description

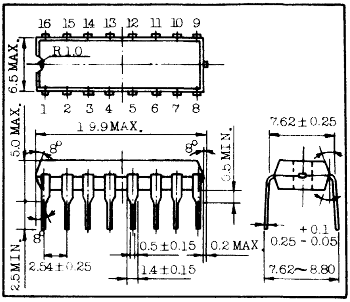
The TD62107P is comprised of four NPN darlington output stages and enable inputs which can gate the outputs. All outputs feature integral clamp diodes for switching inductive loads.
The TD62107P has a wide supply voltage range and all inputs are compatible with TTL and 5V C-MOS.

PIN CONNECTION (TOP VIEW)



PACKAGE

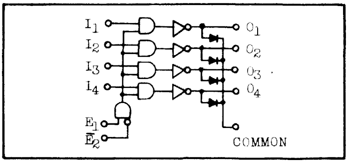
Unit: mm



MAXIMUM RATINGS (Ta=25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	-0.5 ∿ +17	V
Output Sustaining Voltage	$V_{CE(SUS)}$	-0.5 ∿ +45	V
Output Current	I_{OUT}	750	mA
Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
Clamp Diode Reverse Voltage	V_R clamp	45	V
Clamp Diode Forward Current	I_F clamp	500	mA
GND Terminal Current	I_{GND}	3	A
Power Dissipation	P_D	2.7	W
Operating Temperature	T_{opr}	-30 ∿ +75	°C
Storage Temperature	T_{stg}	-55 ∿ +150	°C

BLOCK DIAGRAM

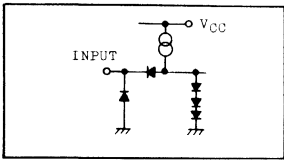


TRUTH TABLE

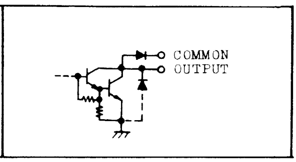
E_1	$\overline{E_2}$	I_1 ～ I_4	O_1 ～ O_4
L	L	L or H	Disable OFF
L	H	L or H	Disable OFF
H	L	L or H	Enable $\overline{I}_n$
H	H	L or H	Disable OFF

$\overline{I}_n = \overline{I}_1 \sim \overline{I}_4$

EQUIVALENT OF INPUTS



EQUIVALENT OF OUTPUTS



TD62107P

RECOMMENDED OPERATING CONDITIONS (Ta=-30~ +75°C)

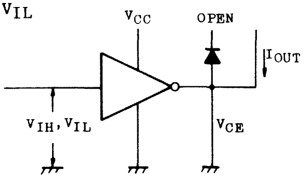
CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}		4.75		15	V
Output Sustaining Voltage	$V_{CE(SUS)}$		0		45	V
Output Current	I_{OUT}	DC 1 Circuit	0		500	mA
		T_{PW}=25ms, D_F=30%, 4 Outputs	0		400	
Input Voltage	V_{IN}		0		V_{CC}	V
Clamp Diode Reverse Voltage	V_{R} clamp				45	V
Clamp Diode Forward Current	I_{F} clamp				500	mA
Power Dissipation	P_D				1.2	W

ELECTRICAL CHARACTERISTICS (Ta=25°C)

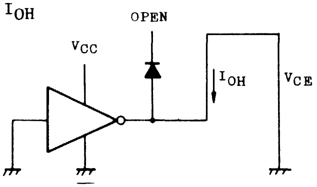
CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
"H" Level Input Voltage		V_{IH}	1		2			V
"L" Level Input Voltage		V_{IL}					0.8	
"H" Level Output Current		I_{OH}	2	V_{CE}=45V, Ta=75°C			100	μA
"L" Level Output Voltage		V_{OL}	3	I_{OUT}=500mA			1.3	V
"H" Level Input Current		I_{IH}	4	V_{IN}=13V			100	μA
"L" Level Input Current		I_{IL}	5	V_{IN}=0.4V			-0.3	mA
Clamp Diode Reverse Current		I_R clamp	6	V_R clamp=45V			100	μA
Clamp Diode Forward Voltage		V_F clamp	7	I_F clamp=500mA			2.0	V
Supply Current	Output OFF	I_{CCH}	4	V_{CC}=13V, V_{IN}=0V OUTPUT OPEN			13	mA
	Output ON	I_{CCL}	5	V_{CC}=13V, V_{IN}=5V OUTPUT OPEN			17	mA
Turn-ON Delay		t_{ON}	8	V_{CC}=5V, R_L=90Ω		5		μs
Turn-OFF Delay		t_{OFF}		C_L=15pF, V_{OUT}=45V		5		

TEST CIRCUIT

1. V_{IH}, V_{IL}

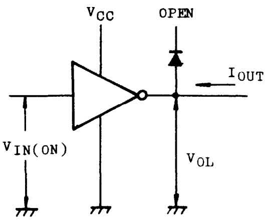


2. I_{OH}

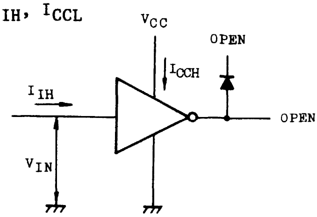


TD62107P

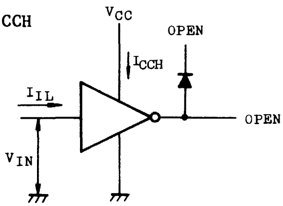
3. V_{OL}



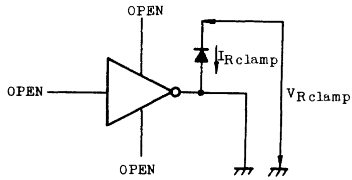
4. I_{IH}, I_{CCL}



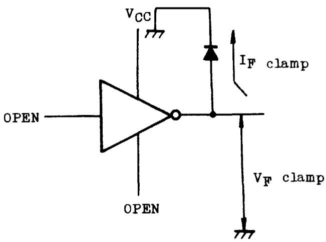
5. I_{IL}, I_{CCH}



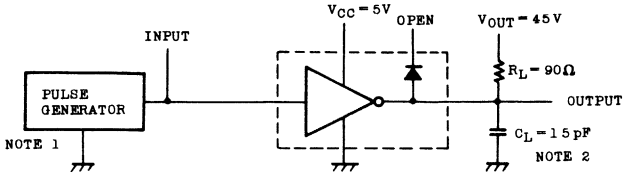
6. I_R clamp



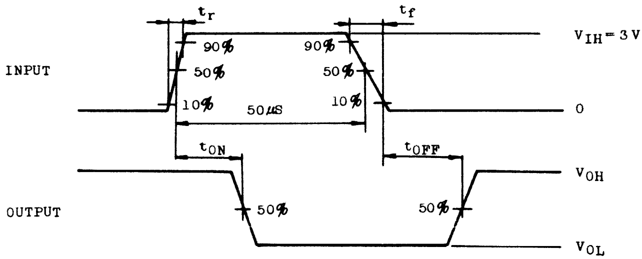
7. V_F clamp



8. t_{ON}, t_{OFF}



TSET CIRCUIT



Notes: 1. Pulse Width 50μS, Duty Cycle 10%
Output Impedance 50Ω, $t_r \leq 5nS$, $t_f \leq 10nS$

2. C_L includes probe and jig capacitance

TD62301P, TD62302P

BIPOLAR DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TD62301P LOW SATURATION DRIVER
TD62302P LOW SATURATION DRIVER

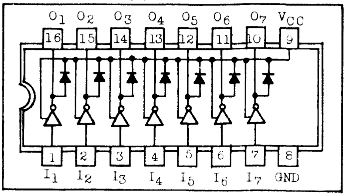
Features

- Low Saturation Outputs $V_{CE}(sat)=0.7V$ Max @ $I_{OUT}=150mA$
- Output Rating 15V/200mA
- Output Clamp Diodes
- Inputs Compatible with TTL and 3∿6V C-MOS

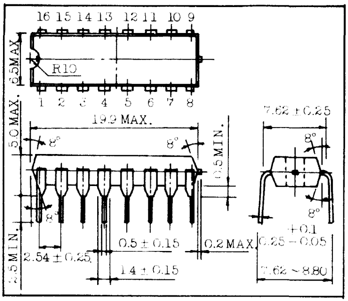
Description

The TD62301P and TD62302P are comprised of seven NPN low saturation drivers.
All units feature integral clamp diodes for switching inductive loads.
These devices are specifically designed for relay, lamp and LED drive in low voltage systems.

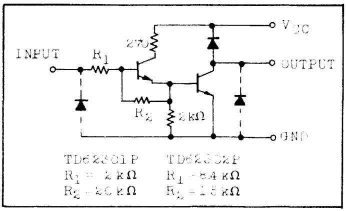
PIN CONNECTION (TOP VIEW)



PACKAGE



SCHEMATICS (EACH DRIVER)



MAXIMUM RATING (Ta=25°C, unless otherwise noted)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Supply Voltage		V_{CC}	−0.5 ∿ +15	V
Output Sustaining Voltage		$V_{CE(SUS)}$	−0.5 ∿ V_{CC} +0.5	V
Output Current		I_{OUT}	200	mA
Input Voltage		V_{IN}	−0.5 ∿ +15	V
Input Current		I_{IN}	15	mA
Clamp Diode	Reverse Voltage	V_R clamp	15	V
	Forward Current	I_F clamp	200	mA
GND Terminal Current		I_{GND}	800	mA
Power Dissipation		P_D	1.0	W
Operating Temperature		T_{opr}	−30 ∿ +75	°C
Storage Temperature		T_{stg}	−55 ∿ +150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=−30∿+75°C)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}		3	5	6	V
Output Current	I_{OUT}	DC 1 Circuit	0		180	mA
		T_{PW}=25mS, D_F=50%, 4 Circuits	0		150	
Input Voltage	V_{IN}		0		V_{CC}	V
Clamp Diode Reverse Voltage	V_R clamp				V_{CC}	V
Clamp Diode Forward Current	I_F clamp				180	mA
Power Dissipation	P_D				0.44	W

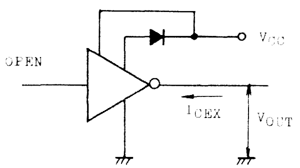
TD62301P, TD62302P

ELECTRICAL CHARACTERISTICS (Ta=25°C)

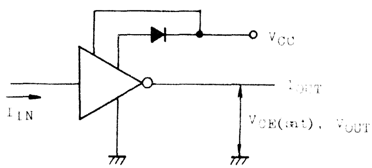
CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Leak Current		I_{CEX}	1	V_{CC}=6V, V_{OUT}=6V, Ta=50°C			7	μA
				V_{CC}=6V, V_{OUT}=6V, Ta=25°C			1	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$	2	V_{CC}=5V, I_{IN}=0.14mA, I_{OUT}=70mA			0.5	V
				V_{CC}=5V, I_{IN}=0.3mA, I_{OUT}=150mA			0.7	
DC Forward Current Transfer Ratio		h_{FE}	2	V_{CC}=5V, V_{OUT}=2V, I_{OUT}=120mA	1000	2000		
Input Current (Output ON)	TD62301P	$I_{IN(ON)}$	3	V_{CC}=5V, V_{IN}=2.4V I_{OUT}=120mA			0.60	mA
	TD62302P						0.14	
Input Voltage (Output ON)	TD62301P	$V_{IN(ON)}$	4	V_{CC}=5V, I_{IN}=0.2mA I_{OUT}=120mA			2.3	V
	TD62302P						4.0	
Clamp Diode Forward Voltage		V_F clamp	5	I_F clamp=120mA			2.0	V
Supply Current		I_{CC}	6	V_{CC}=5V, V_{IN}=5V, I_{OUT}=0		15	22	mA/Gate
Input Capacitance		C_{IN}		V_{IN}=0, f=1MHz		15		pF
Turn-ON Delay		t_{ON}	7	V_{CC}=6V, R_L=33Ω C =15pF		0.1		μs
Turn-OFF Delay		t_{OFF}				0.2		

TEST CIRCUIT

1. I_{CEX}

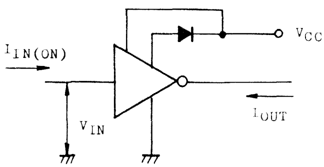


2. h_{FE}, V_{CE}(sat)

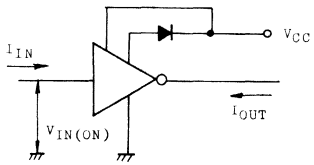


$$h_{FE}=\frac{I_{OUT}}{I_{IN}}$$

3. I_{IN}(ON)

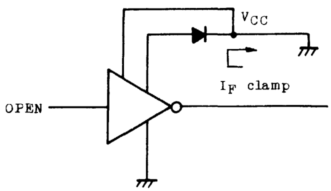


4. V_{IN}(ON)

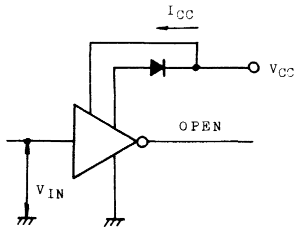


TD62301P, TD62302P

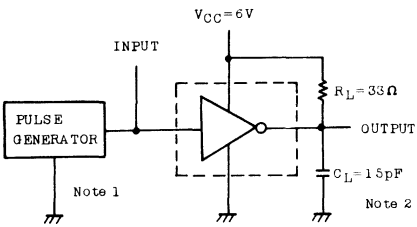
5. V_F clamp

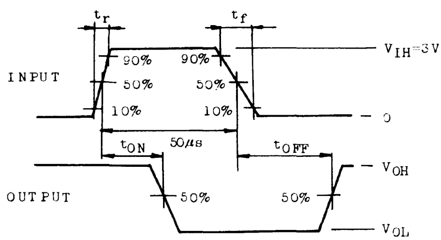


6. I_{CC}



7. t_{ON}, t_{OFF}

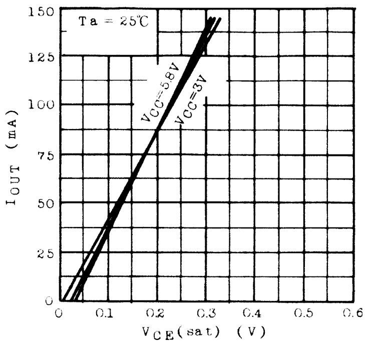




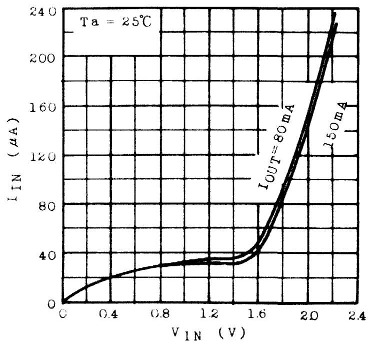
Notes: 1. Pulse Width 50μS, Duty Cycle 10%
Output Impedance 50Ω
$t_r \leqq 5nS$, $t_f \leqq 10nS$

2. C_L includes probe and jig capacitance.

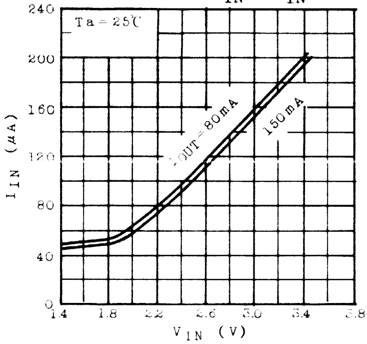
I_{OUT} - $V_{CE}(sat)$



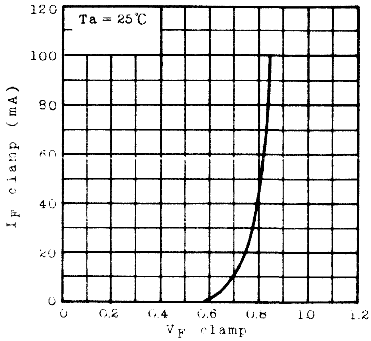
TD62301P I_{IN} - V_{IN}



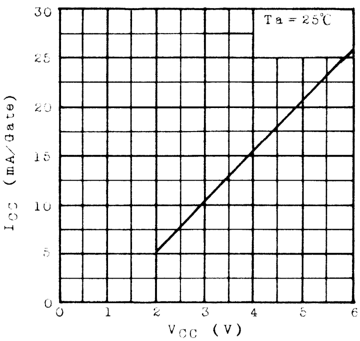
TD62302P I_{IN} - V_{IN}



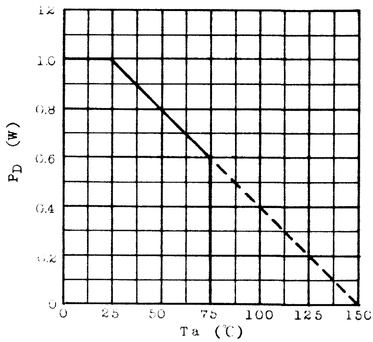
I_F clamp - V_F clamp



I_{CC} - V_{CC}



P_D - Ta



TD62303P

BIPOLAR DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TD62303P 6 DIGIT DRIVER

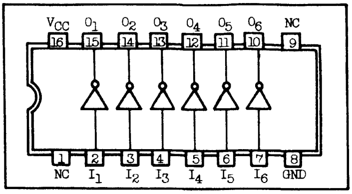
Features

- Output Current .... 500mA Max.
- Output Voltage 17V
- TTL, C-MOS Compatible Inputs
- Suitable for Digit-Driver of 6 Digit Common Cathode LED Displays

Description

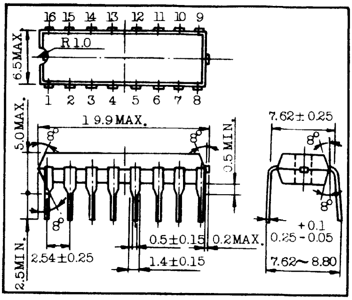
The TD62303P is comprised of six NPN low saturation drivers.
This device is specifically designed for multiplexed digit driving of six digits common cathode LED displays.
The TD62303P is intended for use with TTL and 5V C-MOS.

PIN CONNECTION (TOP VIEW)



PACKAGE

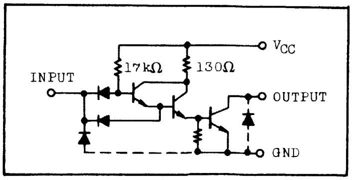
Unit: mm



MAXIMUM RATINGS (Ta=25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	-0.5 ∿ +7.0	V
Output Sustaining Voltage	$V_{CE(SUS)}$	-0.5 ∿ +17	V
Output Current	I_{OUT}	500	mA
Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
Input Current	I_{IN}	-10	mA
GND Terminal Current	I_{GND}	1.0	A
Power Dissipation	P_D	1.0	W
Operating Temperature	T_{opr}	-30 ∿ +75	°C
Storage Temperature	T_{stg}	-55 ∿ +150	°C

SCHEMATICS (EACH DRIVER)



RECOMMENDED OPERATING CONDITIONS (Ta=-30 ∿ +75°C)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
Output Sustaining Voltage	$V_{CE(SUS)}$		0		15	V
Output Current	I_{OUT}	DC 1 Circuit	0		350	mA
Input Voltage	V_{IN}		0		V_{CC}	V
Power Dissipation	P_D				0.44	W

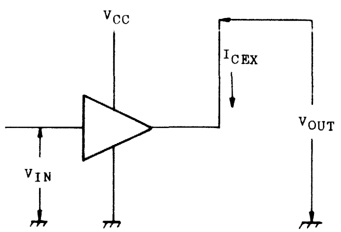
TD62303P

ELECTRICAL CHARACTERISTICS (Ta=25°C)

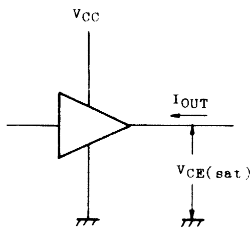
CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Leak Current	I_{CEX}	1	V_{CC}=5.5V, V_{IN}=0V V_{OUT}=15V, Ta=75°C			100	μA
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	2	V_{CC}=4.5V, I_{OUT}=150mA		0.3	0.4	V
			V_{CC}=4.5V, I_{OUT}=350mA		0.65	0.8	
Input Current (Output ON)	$I_{IN(ON)}$	3	V_{CC}=5.5V, V_{IN}=5.5V			40	μA
Input Current (Output OFF)	$I_{IN(OFF)}$	4	V_{CC}=5.5V, V_{IN}=0.4V			-0.36	mA
Input Voltage (Output ON)	$V_{IN(ON)}$	5				2.0	V
Input Voltage (Output OFF)	$V_{IN(OFF)}$	5		0.8			V
Supply Current	I_{CC}	6	V_{CC}=5.5V, V_{IN}=5.5V			47	mA/Gate
Turn-ON Delay	t_{ON}	7	V_{CC}=5.0V, R_L=42Ω V_{OUT}=15V, C_L=15pF				μs
Turn-OFF Delay	t_{OFF}						

TEST CIRCUIT

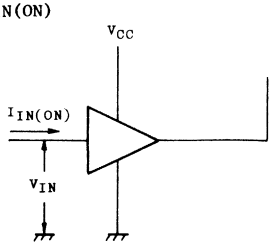
1. I_{CEX}



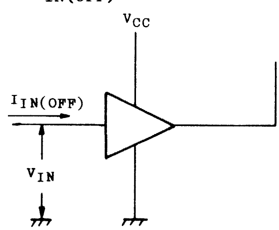
2. $V_{CE(sat)}$



3. $I_{IN(ON)}$

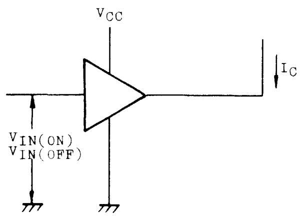


4. $I_{IN(OFF)}$

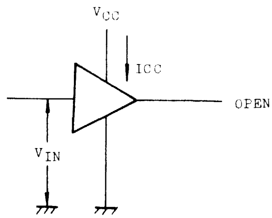


TD62303P

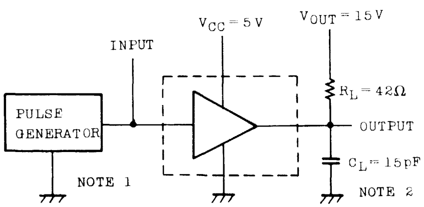
5. $V_{IN}(ON)$, $V_{IN}(OFF)$

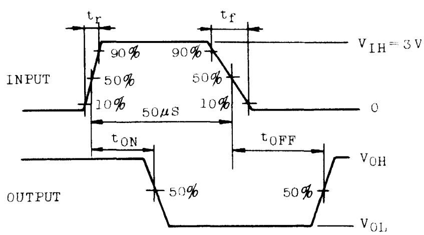


6. I_{CC}



7. t_{ON}, t_{OFF}





NOTE 1 Pulse width=50μs, Duty Cycle=10%
Zo=50Ω, $t_r \leqq 5$nS, $t_f \leqq 10$nS

NOTE 2 C_L includes all probe and jig capacitance.

BIPOLAR DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TD62304AP, TD62305AP

TENTATIVE

TD62304AP LOW INPUT ACTIVE DRIVER
TD62305AP LOW INPUT ACTIVE DRIVER

Features

- Output Current....................500mA Max.
- High Sustaining Voltage ....50V Min.
- Low Level Active Inputs

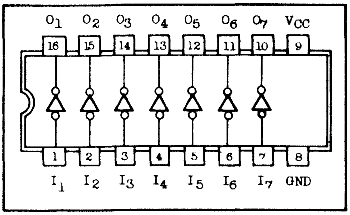
TYPE	$V_{IN(ON)}$
TD62304AP	$-20V \sim V_{CC}-2.8V$
TD62305AP	$0V \sim V_{CC}-3.7V$

- TTL, C-MOS Compatible Inputs
- Standard Supply Voltage

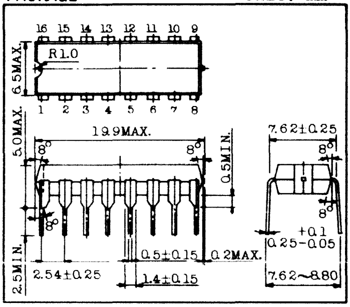
Description

The TD62304AP and TD62305AP are non-inverting transistor arrays, which are comprised of seven NPN darlington output stages and PNP input stages. These devices are Low Level input active drivers and are suitable for operations with TTL, 5V C-MOS and 5V Microprocessor which have sink current output drivers.

PIN CONNECTION (TOP VIEW)



PACKAGE Unit: mm

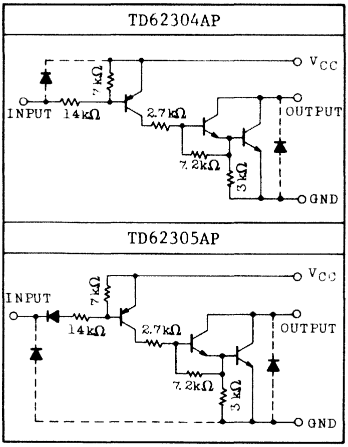


MAXIMUM RATINGS (Ta=25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	$-0.5\sim+7.0$	V
Output Sustaining Voltage	$V_{CE(SUS)}$	50	V
Output Current	I_{OUT}	500	mA
Input Voltage	V_{IN} *	$-22\sim V_{CC}+0.5$	V
	V_{IN} **	$-0.5\sim7$	
Input Current	I_{IN}	-10	mA
GND Terminal Current	I_{GND}	2.5	A
Power Dissipation	P_D	1.47	W
Operating Temperature	T_{opr}	$-40\sim+85$	°C
Storage Temperature	T_{stg}	$-55\sim+150$	°C

* TD62304AP
** TD62305AP

SCHEMATICS (EACH DRIVER)



TD62304AP, TD62305AP

RECOMMENDED OPERATING CONDITIONS (Ta=−40～+85°C)

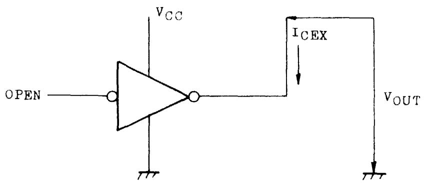
CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage		V_{CC}		4.5	5.0	5.5	V
Output Sustaining Voltage		$V_{CE(SUS)}$		0		50	V
Output Current		I_{OUT}	T_{PW}=25ms, D_F=8%, 7 Circuits	0		350	mA
			T_{PW}=25ms, D_F=20%, 7 Circuits	0		200	
Input Voltage	TD62304AP	V_{IN}		−20		V_{CC}	V
	TD62305AP			0		5.5	
Power Dissipation		P_D				0.52	W

ELECTRICAL CHARACTERISTICS (Ta=25°C)

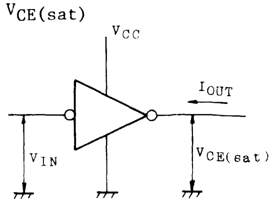
CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Leak Current		I_{CEX}	1	V_{CC}=5.5V, I_{IN}=0 V_{OUT}=50V, Ta=85°C			100	μA
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$	2	V_{CC}=4.5V, V_{IN}=$V_{IN(ON)}$Max. I_{OUT}=350mA		1.4	2.0	V
Input Current (Output ON)	TD62304AP	$I_{IN(ON)}$	3	V_{CC}=5.5V, V_{IN}=0.4V		−0.32	−0.45	mA
	TD62305AP			V_{CC}=5.5V, V_{IN}=−20V			−2.6	
Input Current (Output OFF)		$I_{IN(OFF)}$	4				−40	μA
Input Voltage	TD62304AP	$V_{IN(ON)}$	5		−20		V_{CC}−2.8	V
	TD62305AP				0		V_{CC}−3.7	
Supply Current		$I_{CC(ON)}$	6	V_{CC}=5.5V, V_{IN}=0V		17	22	mA
		$I_{CC(OFF)}$		V_{CC}=5.5V, V_{IN}=V_{CC}			100	μA
Turn-ON Delay		t_{ON}	7	V_{CC}=5V, V_{OUT}=50V		0.1		μs
Turn-OFF Delay		t_{OFF}		R_L=163Ω, C_L=15pF		3		

TEST CIRCUIT

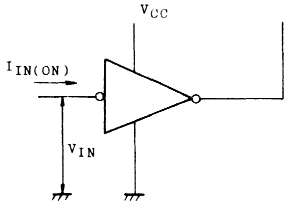
1. I_{CEX}



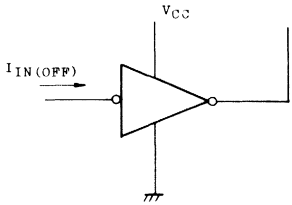
2. $V_{CE(sat)}$



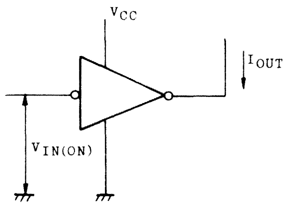
3. $I_{IN(ON)}$



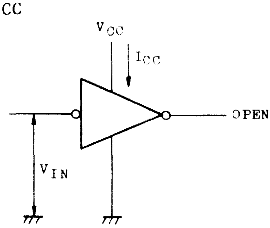
4. $I_{IN(OFF)}$



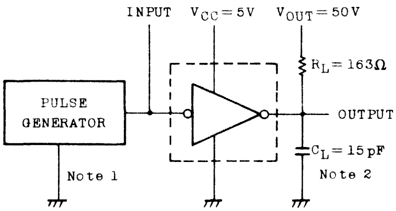
5. $V_{IN(ON)}$

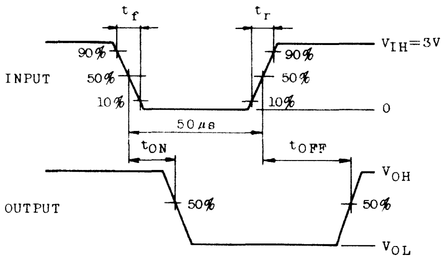


6. I_{CC}



7. t_{ON}, t_{OFF}

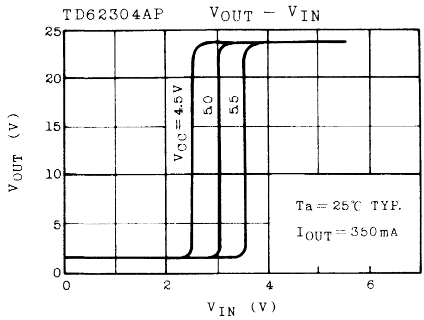


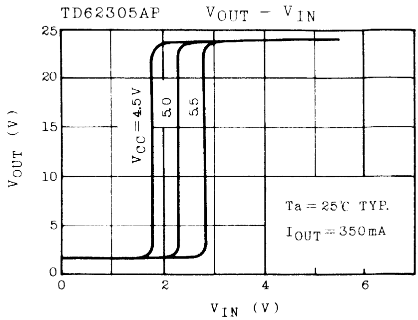


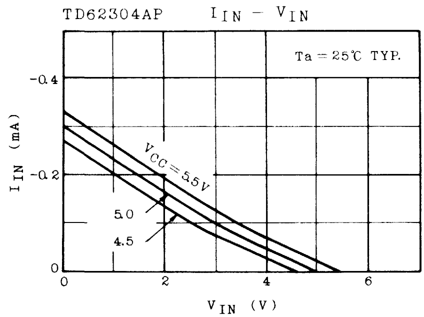
Notes: 1. Pulse Width 50μs, Duty Cycle 10%
Output Impedance 50Ω, $t_r \leqq 5ns$, $t_f \leqq 10ns$

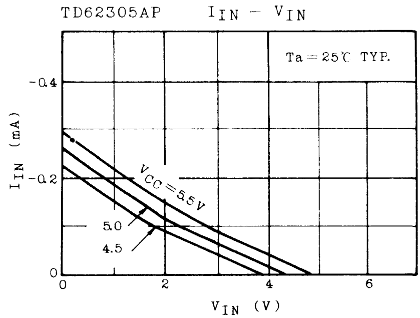
2. C_L includes probe and jig capacitance

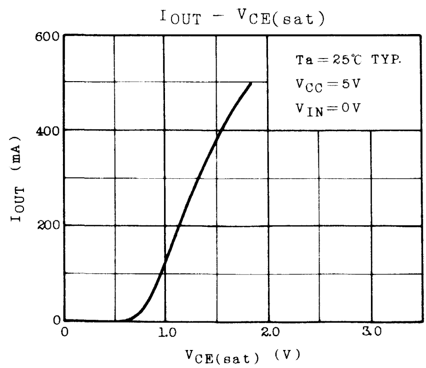
TD62304AP, TD62305AP

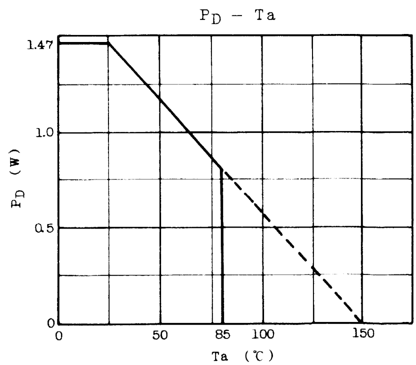












BIPOLAR DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TD62306P

TD62306P LOW SATURATION DRIVER

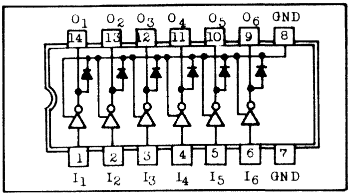
Features

- Low Saturation Outputs $V_{CE}(sat)$=0.6V Max. @ I_{OUT}=120mA
- Output Rating 20V/150mA
- Output Clamp Diodes
- Inputs Compatible with 5∿15V P-MOS, C-MOS
- Input Protective Diodes against a Negative Input Voltage

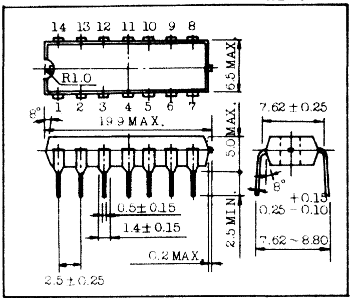
Description

The TD62306P is comprised of six NPN low saturation drivers. All units feature integral clamp diodes for switching inductive loads and protective diodes against a negative input voltage.

PIN CONNECTION (TOP VIEW)



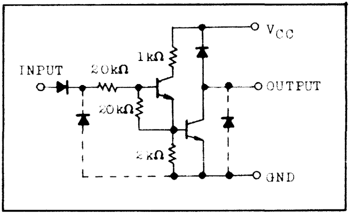
PACKAGE Unit: mm



MAXIMUM RATINGS (Ta=25°C, unless otherwise noted)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Supply Voltage		V_{CC}	−0.5 ∿ +20	V
Output Sustaining Voltage		$V_{CE}(SUS)$	−0.5 ∿ V_{CC} + 0.5	V
Output Current		I_{OUT}	150	mA
Input Voltage		V_{IN}	−37 ∿ +20	V
Input Current		I_{IN}	1.5	mA
Clamp Diode	Reverse Voltage	V_R clamp	20	V
	Forward Current	I_F clamp	120	mA
GND Terminal Current		I_{GND}	800	mA
Power Dissipation		P_D	1.0	W
Operating Temperature		T_{opr}	−30 ∿ +75	°C
Storage Temperature		T_{stg}	−55 ∿ +150	°C

SCHEMATICS (EACH DRIVER)



RECOMMENDED OPERATING CONDITIONS (Ta=−30∿+75°C)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}		4.75		18	V
Output Current	I_{OUT}	DC 1 Circuit	0		120	mA
		T_{PW}=25ms, D_F=10% 6 Circuits	0		100	
Input Voltage	V_{IN}		−35		V_{CC}	V
Clamp Diode Reverse Voltage	V_R clamp				18	V
Clamp Diode Forward Current	I_F clamp				120	mA
Power Dissipation	P_D				0.44	W

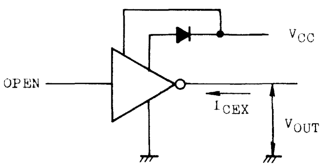
TD62306P

ELECTRICAL CHARACTERISTICS (Ta=25°C)

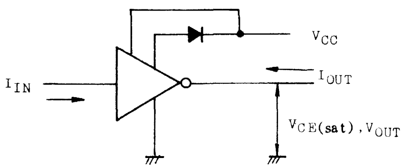
CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Leak Current		I_{CEX}	1	V_{CC}=18V, V_{OUT}=18V, Ta=75°C			100	μA
Collector - Emitter Saturation Voltage		V_{CE}(sat)	2	V_{CC}=5V, I_{IN}=0.2mA, I_{OUT}=120mA		0.45	0.6	V
DC Forward Current Transfer Ratio		h_{FE}	2	V_{CC}=5V, V_{OUT}=2V, I_{OUT}=120mA	1000			
Input Current	Output ON	I_{IN}(ON)	3	V_{IN}=5V, I_{OUT}=120mA		0.16	0.23	mA
				V_{IN}=15V, I_{OUT}=120mA		0.66	0.94	
	Output OFF	I_{IN}(OFF)	4	V_{IN}=-35V			-10	μA
Clamp Diode Forward Voltage		V_F clamp	5	I_F clamp=120mA		1.25	1.6	V
Supply Current	Output ON	I_{CC}(ON)	6	V_{CC}=V_{IN}=5V		4.0	6.0	mA/Gate
				V_{CC}=V_{IN}=15V		14.0	22	
	Output OFF	I_{CC}(OFF)	6	V_{CC}=18V, V_{IN}=0V			10	μA
Turn-ON Delay		t_{ON}	7	V_{CC}=18V, R_L=150Ω		0.1		μs
Turn-OFF Delay		t_{OFF}		C_L=150pF		0.8		

TEST CIRCUIT

1. I_{CEX}

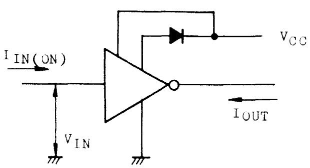


2. h_{FE}, V_{CE}(sat)

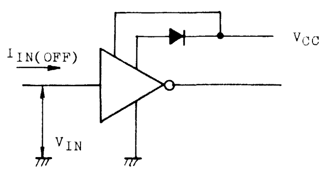


$h_{FE} = \frac{I_{OUT}}{I_{IN}}$

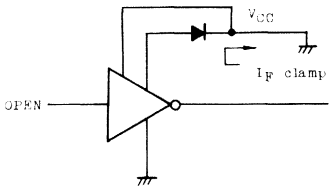
3. I_{IN}(ON)



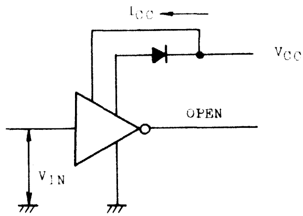
4. I_{IN}(OFF)



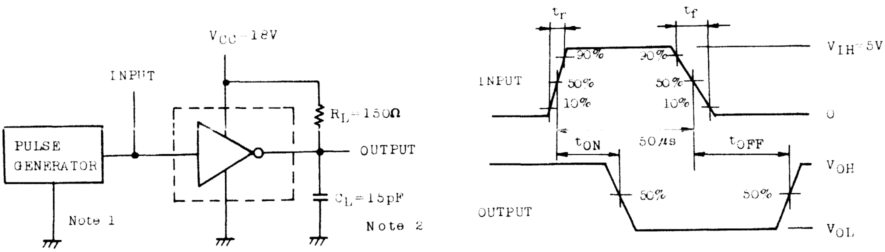
5. V_F clamp



6. I_{CC}



7. t_{ON}, t_{OFF}



Notes: 1. Pulse Width 50μS, Duty Cycle 10%

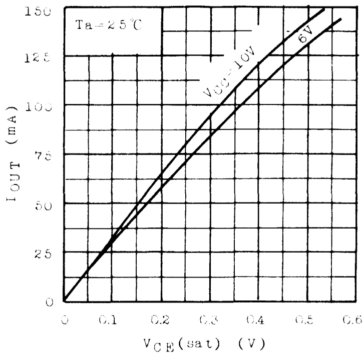
Output Impedance 50Ω

$t_r \leq 5nS$, $t_f \leq 10nS$

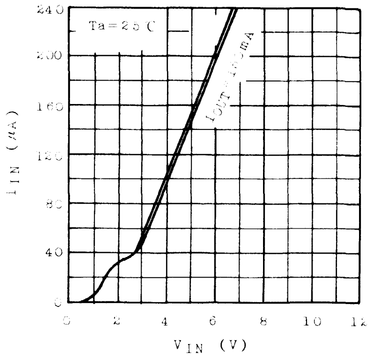
2. C_L includes probe and jig capacitance.

TD62306P

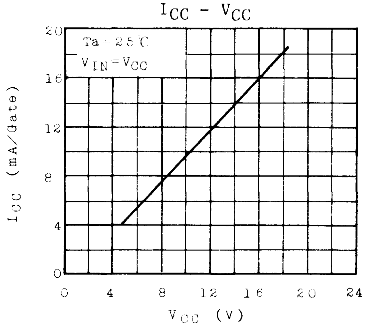
I_{OUT} - V_{CE}(sat)



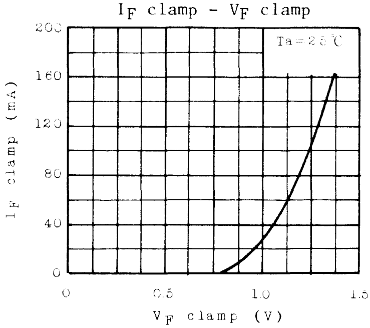
I_{IN} - V_{IN}



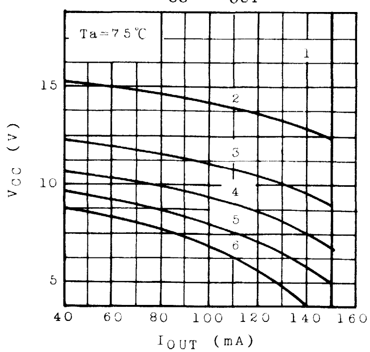
I_{CC} - V_{CC}



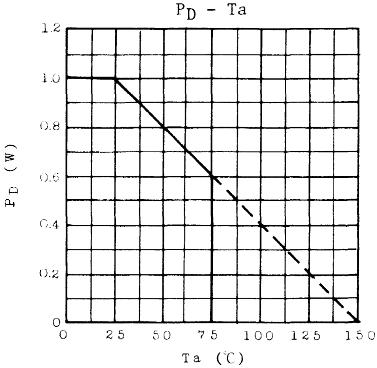
I_F clamp - V_F clamp



V_{CC} - I_{OUT}



P_D - Ta



BIPOLAR DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TD62307P

TD62307P LOW SATURATION DRIVER

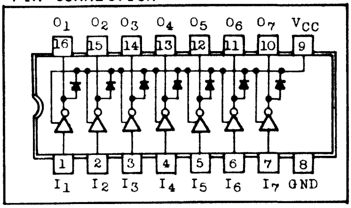
Features

- Low Saturation Outputs $V_{CE(sat)}$=0.6V Max. @I_{OUT}=120mA
- Output Rating 20V/150mA
- Output Clamp Diodes
- Inputs Compatible with 5∿15V P-MOS, C-MOS
- Input Protective Diodes against a Negative Input Voltage

Description

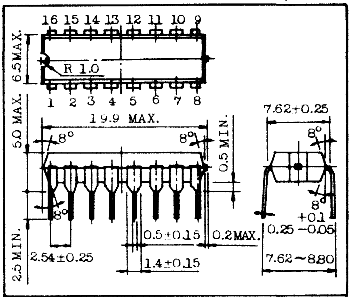
The TD62307P is comprised of six NPN low saturation drivers. All units feature integral clamp diodes for switching inductive loads and protective diodes against a negative input voltage.

PIN CONNECTION (TOP VIEW)

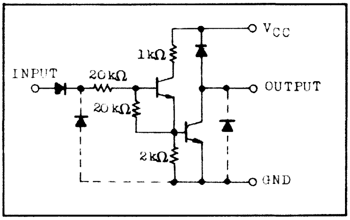


PACKAGE

Unit: mm



SCHEMATICS (EACH DRIVER)



MAXIMUM RATINGS (Ta=25°C, unless otherwise noted)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Supply Voltage		V_{CC}	−0.5 ∿ +20	V
Output Sustaining Voltage		$V_{CE(SUS)}$	−0.5 ∿ V_{CC} +0.5	V
Output Current		I_{OUT}	150	mA
Input Voltage		V_{IN}	−37 ∿ +20	V
Input Current		I_{IN}	1.5	mA
Clamp Diode	Reverse Voltage	V_R clamp	20	V
	Forward Current	I_F clamp	120	mA
GND Terminal Current		I_{GND}	800	mA
Power Dissipation		P_D	1.0	W
Operating Temperature		T_{opr}	−30 ∿ +75	°C
Storage Temperature		T_{stg}	−55 ∿ +150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=−30 ∿ +75°C)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}		4.75		18	V
Output Current	I_{OUT}	DC 1 Circuit	0		120	mA
		T_{PW}=25ms, D_F=10% 7 Circuits	0		100	
Input Voltage	V_{IN}		−35		V_{CC}	V
Clamp Diode Reverse Voltage	V_R clamp				18	V
Clamp Diode Forward Current	I_F clamp				120	mA
Power Dissipation	P_D				0.44	W

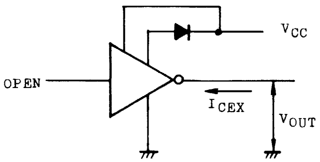
TD62307P

ELECTRICAL CHARACTERISTICS (Ta=25°C)

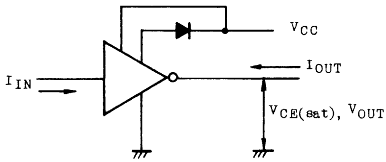
CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Leak Current		I_{CEX}	1	V_{CC}=18V, V_{OUT}=18V, Ta=75°C			100	μA
Collector - Emitter Saturation Voltage		$V_{CE(sat)}$	2	V_{CC}=5V, I_{IN}=0.2mA, I_{OUT}=120mA		0.45	0.6	V
DC Forward Current Transfer Ratio		h_{FE}	2	V_{CC}=5V, V_{OUT}=2V, I_{OUT}=120mA	1000			
Input Current	Output ON	$I_{IN(ON)}$	3	V_{IN}=5V, I_{OUT}=120mA		0.16	0.23	mA
				V_{IN}=15V, I_{OUT}=120mA		0.66	0.94	
	Output OFF	$I_{IN(OFF)}$	4	V_{IN}=−35V			−10	μA
Clamp Diode Forward Voltage		V_{F} clamp	5	I_F clamp=120mA		1.25	1.6	V
Supply Current	Output ON	$I_{CC(ON)}$	6	V_{CC}=V_{IN}=5V		4.0	6.0	mA/Gate
				V_{CC}=V_{IN}=15V		14.0	22	
	Output OFF	$I_{CC(OFF)}$	6	V_{CC}=18V, V_{IN}=0V			10	μA
Turn-ON Delay		t_{ON}	7	V_{CC}=18V, R_L=150Ω C_L=150pF		0.1		μs
Turn-OFF Delay		t_{OFF}				0.8		

TEST CIRCUIT

1. I_{CEX}

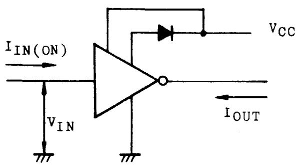


2. h_{FE}, $V_{CE(sat)}$

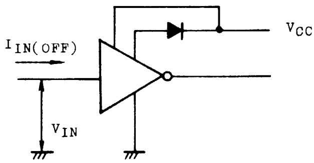


$$h_{FE} = \frac{I_{OUT}}{I_{IN}}$$

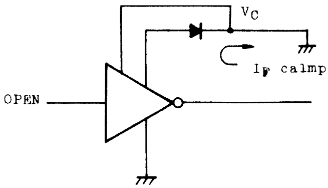
3. $I_{IN(ON)}$



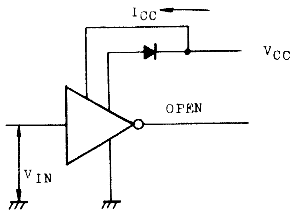
4. $I_{IN(OFF)}$



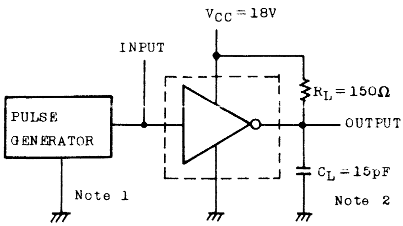
5. V_F clamp

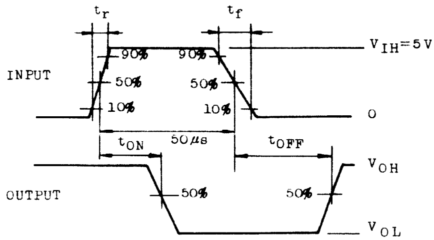


6. I_{CC}



7. t_{ON}, t_{OFF}

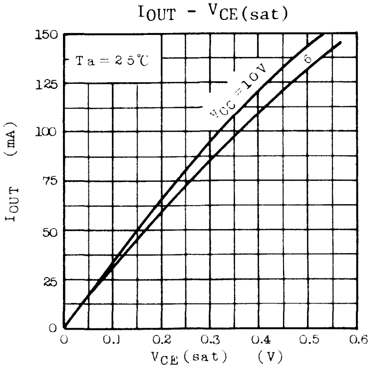


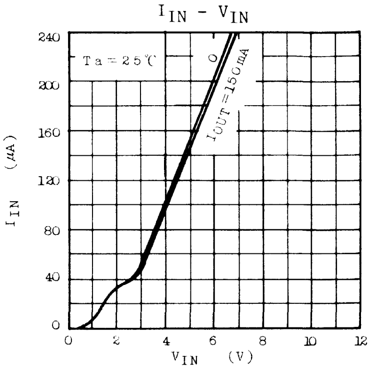


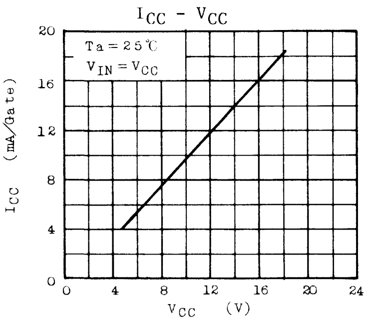
Notes: 1. Pulse Width 50μS, Duty Cycle 10%
Output Impedance 50Ω
$t_r \leq 5nS$, $t_f \leq 10nS$

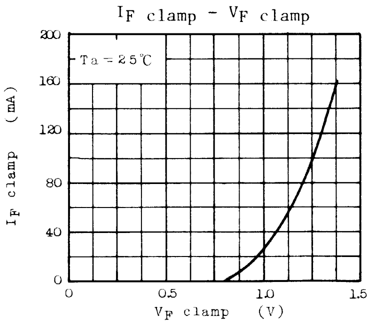
2. C_L includes probe and jig capacitance.

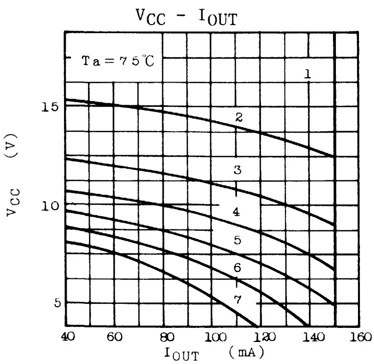
TD62307P

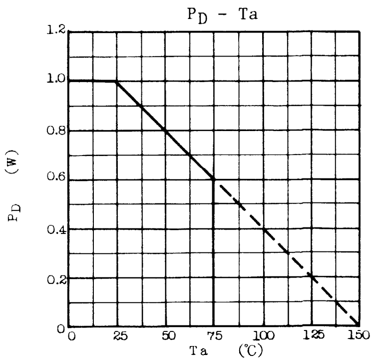

IOUT - VCE(sat)
Ta = 25°C
VCC = 10V
6
IOUT (mA)
VCE(sat) (V)
150
125
100
75
50
25
0
0
0.1
0.2
0.3
0.4
0.5
0.6


IIN - VIN
Ta = 25°C
0
IOUT = 150mA
IIN (μA)
VIN (V)
240
200
160
120
80
40
0
0
2
4
6
8
10
12


ICC - VCC
Ta = 25°C
VIN = VCC
ICC (mA/Gate)
VCC (V)
20
16
12
8
4
0
0
4
8
12
16
20
24


IF clamp - VF clamp
Ta = 25°C
IF clamp (mA)
VF clamp (V)
200
160
120
80
40
0
0
0.5
1.0
1.5


VCC - IOUT
Ta = 75°C
1
2
3
4
5
6
7
VCC (V)
IOUT (mA)
15
10
5
40
60
80
100
120
140
160


PD - Ta
PD (W)
Ta (°C)
1.2
1.0
0.8
0.6
0.4
0.2
0
0
25
50
75
100
125
150

BIPOLAR DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TD62308AP

TENTATIVE

TD62308AP LOW INPUT ACTIVE 1.5A DRIVER

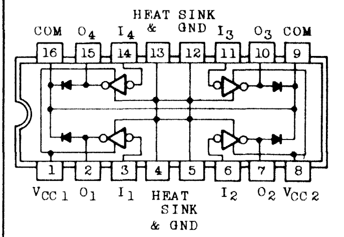
Features

- Output Current..................1.5A Max.
- High Sustaining Voltage ....50V Min.
- Low Level Active Inputs
- TTL and C-MOS Compatible Inputs
- Standard Supply Voltage
- Two V_{CC} Terminals V_{CC1}, V_{CC2} (Separated)

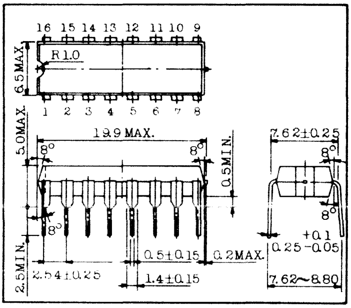
Description

The TD62308AP is a non-inverting transistor array, which is comprised of four NPN darlington output stages and PNP input stages.
This device is low level input active driver and is suitable for operation with TTL, 5V C-MOS and 5V Microprocessor which have sink current output drivers.

PIN CONNECTION (TOP VIEW)



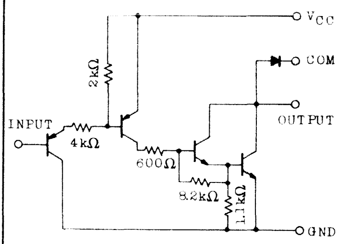
PACKAGE Unit: mm



MAXIMUM RATINGS (Ta=25°C unless otherwise noted)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Supply Voltage		V_{CC}	-0.5 ~ 10	V
Output Sustaining Voltage		$V_{CE(SUS)}$	-0.5 ~ +50	V
Output Current		I_{OUT}	1.5	A
Input Current		I_{IN}	-10	mA
Input Voltage		V_{IN}	-0.5 ~ +30	V
Clamp Diode	Reverse Voltage	V_R	50	V
	Forward Current	I_F	1.5	A
Common Terminal Current		I_{COM}	3.0	A
GND Terminal Current		I_{GND}	5.0	A
Power Dissipation		P_D	2.7	W
Operating Temperature		T_{opr}	-40 ~ +85	°C
Storage Temperature		T_{stg}	-55 ~ +150	°C

SCHEMATICS (EACH DRIVER)



TD62308AP

RECOMMENDED OPERATING CONDITION (Ta=-40~ +85°C)

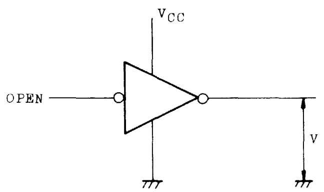
CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}		4.5		5.5	V
Output Sustaining Voltage	$V_{CE(SUS)}$		0		50	V
Output Current	I_{OUT}		0		1.25	A
Input Voltage	V_{IN}		0		25	V
Clamp Diode Reverse Voltage	V_R		0		50	V
Clamp Diode Froward Current	I_F		0		1.25	A
Power Dissipation	P_D		0		1.0	W

ELECTRICAL CHARACTERISTICS (Ta=25°C unless otherwise noted)

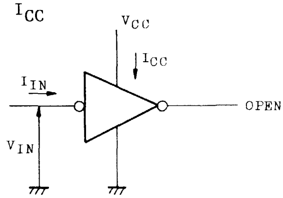
CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
"H" Level Input Voltage	V_{IH}	-		V_{CC} -1.6		25	V
"L" Level Input Voltage	V_{IL}	-		0		V_{CC} -3.6	V
"H" Level Input Current	I_{IH}	2				10	μA
"L" Level Input Current	I_{IL}	2	V_{CC}=5.5V, V_{IN}=0.4V		-0.05	-0.36	mA
Output Leak Current	I_{CEX}	1	V_{OUT}=50V, Ta=85°C			100	μA
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	3	V_{CC}=4.5V, I_{OUT}=1.25A		1.3		V
			V_{CC}=4.5V, I_{OUT}=0.7A				
Clamp Diode Reverse Current	I_R	4	V_R=50V			50	μA
Clamp Diode Forward Voltage	V_F	5	I_F=1.25A		1.5		V
Supply Current	$I_{CC(ON)}$	2	V_{CC}=5.5V, V_{IN}=0V		35		mA
	$I_{CC(OFF)}$	2	V_{CC}=5.5V, V_{IN}=V_{CC}			10	μA
Turn-ON Delay	t_{ON}	6	V_{CC}=5.0V, R_L=43Ω				μs
Turn-OFF Delay	t_{OFF}		V_{OUT}=50V, C_L=15pF				

TEST CIRCUIT

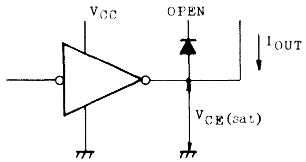
1. I_{CEX}



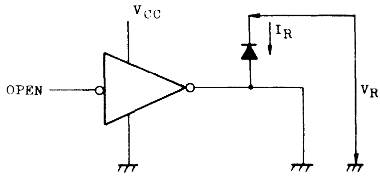
2. I_{CC}



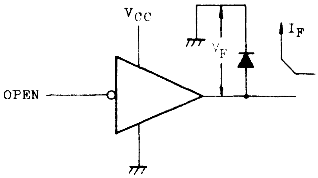
3. $V_{CE(sat)}$



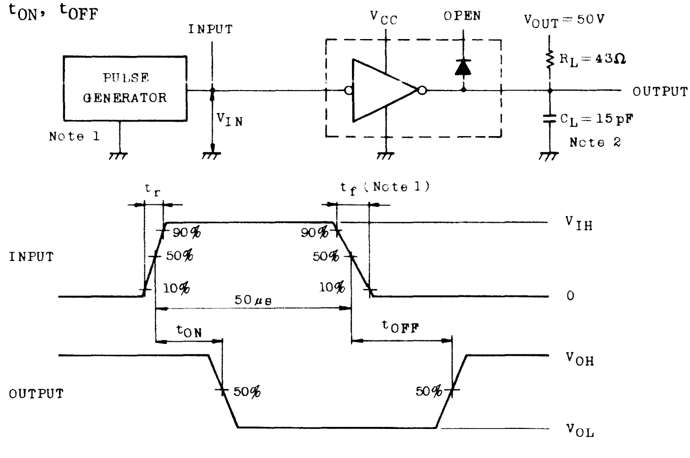
4. I_R



5. V_F



6. t_{ON}, t_{OFF}



Notes: 1. Pulse Width 50μs, Duty Cycle 10%
Output Impedance 50Ω
$t_r \leqq 5ns$, $t_f \leqq 10ns$

2. C_L includes probe and jig capacitance.

TD62476P, TD62477P TD62478P, TD62479P

BIPOLAR DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TD62476P DUAL PERIPHERAL AND DRIVER
TD62477P DUAL PERIPHERAL NAND DRIVER
TD62478P DUAL PERIPHERAL OR DRIVER
TD62479P DUAL PERIPHERAL NOR DRIVER

Features

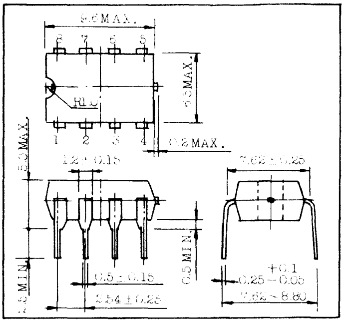
- Output Current .... 350mA Max.
- High Sustaining Voltage..35V
- Output clamp Diodes
- Inputs Compatible with TTL and 5V C·MOS
- Standard Supply Voltage

TD62476P			TD62477P			TD62478P			TD62479P		
INPUT		OUTPUT	INPUT		OUTPUT	INPUT		OUTPUT	INPUT		OUTPUT
C_{IN}	I		C_{IN}	I		C_{IN}	I		C_{IN}	I	
0	0	ON	0	0	OFF	0	0	ON	0	0	OFF
0	1	ON	0	1	OFF	0	1	OFF	0	1	ON
1	0	ON	1	0	OFF	1	0	OFF	1	0	ON
1	1	OFF	1	1	ON	1	1	OFF	1	1	ON

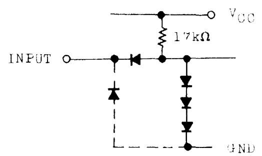
MAXIMUM RATINGS (Ta=25°C, unless otherwise noted)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Supply Voltage		V_{CC}	-0.5 ∿ +7.0	V
Input Voltage		V_{IN}	-0.5 ∿ +5.5	V
Output Sustaining Voltage		$V_{CE(SUS)}$	-0.5 ∿ +35	V
Output Current		I_{OUT}	350	mA
Clamp Diode	Reverse Voltage	V_R clamp	35	V
	Forward Current	I_F clamp	300	mA
Power Dissipation		P_D	0.9	W
Operating Temperature		T_{opr}	-30 ∿ +75	°C
Storage Temperature		T_{stg}	-55 ∿ +150	°C

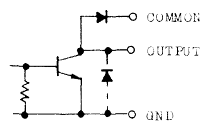
PACKAGE Unit: mm



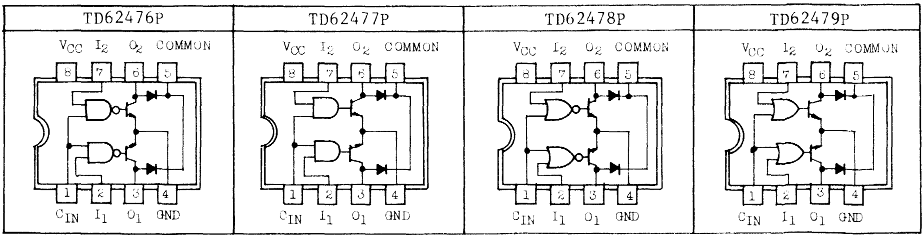
EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



PIN CONNECTIONS (TOP VIEW)



TD62476P, TD62477P
TD62478P, TD62479P

RECOMMENDED OPERATING CONDITIONS (Ta=-30 ∿ +75°C)

CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage		V_{CC}		4.5	5.0	5.5	V
Output Sustaining Voltage		$V_{CE(SUS)}$		0		35	V
Output Current		I_{OUT}	1 Circuit	0		300	mA
			2 Circuits	0		200	
Input Voltage		V_{IN}		0		V_{CC}	V
Clamp Diode	Reverse Voltage	$V_{R\ clamp}$				35	V
	Forward Current	$I_{F\ clamp}$				300	mA
Power Dissipation		P_D				0.4	W

ELECTRICAL CHARACTERISTICS (Ta=25°C)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
"H" Level Input Voltage		V_{IH}	1			2.0			V
"L" Level Input Voltage		V_{IL}	1					0.8	V
"H" Level Output Current		I_{OH}	2	V_{CC}=4.5V, V_{IH}=2.0V V_{IL}=0.8V, V_{OH}=35V				10	μA
"L" Level Output Voltage		V_{OL}	3	V_{CC}=4.5V	I_{OL}=100mA		0.15	0.30	V
				V_{IH}=2.0V	I_{OL}=200mA		0.28	0.45	
				V_{IL}=0.8V	I_{OL}=300mA		0.45	0.60	
"H" Level Input Current		I_{IH}	4	V_{CC}=5.5V, V_{IN}=5.5V				10	μA
"L" Level Input Current		I_{IL}	5	V_{CC}=5.5V, V_{IN}=0.4V			-0.26	-0.4	mA
							-0.52	-0.8	
Clamp Diode	Reverse Current	$I_{R\ clamp}$	6	V_{CC}=4.5V, V_R=35V				10	μA
	Forward Voltage	$V_{F\ clamp}$	7	V_{CC}=4.5V, I_F=300mA			1.5	1.75	V
Supply Current Output "H" (OFF)	TD62476P	I_{CCH}	5	V_{CC}=5.5V	V_{IN}=5V		8.4	14	mA
	TD62477P				V_{IN}=0V		0.6	0.85	
	TD62478P				V_{IN}=5V		9	14	
	TD62479P				V_{IN}=0V		1.1	1.8	
Supply Current Output "L" (ON)	TD62476P	I_{CCL}	4	V_{CC}=5.5V	V_{IN}=5V		38	55	mA
	TD62477P				V_{IN}=0V		36	53	
	TD62478P				V_{IN}=5V		39	56	
	TD62479P				V_{IN}=0V		36	53	

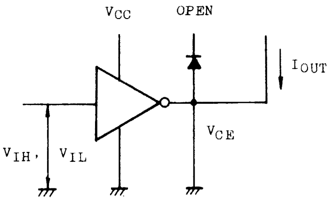
TD62476P, TD62477P
TD62478P, TD62479P

SWITCHING CHARACTERISTICS (Ta=25°C)

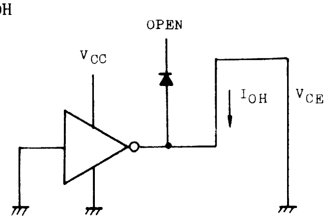
CHARACTERISTIC		SYMBOL	CONDITION	TD62476P MIN.	TD62476P TYP.	TD62476P MAX.	TD62477P MIN.	TD62477P TYP.	TD62477P MAX.	TD62478P MIN.	TD62478P TYP.	TD62478P MAX.	TD62479P MIN.	TD62479P TYP.	TD62479P MAX.	UNIT
Propagation Delay Time	"L"-"H"	t_{pLH}	C_L=15pF R_L=120Ω		0.7			0.7			0.7			0.7		μS
	"H"-"L"	t_{pHL}			0.2			0.2			0.2			0.2		
Rise Time		t_{or}														
Fall Time		t_{of}														

TEST CIRCUIT

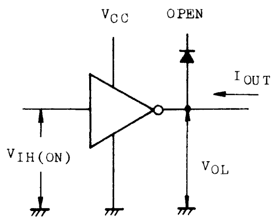
1. V_{IH}, V_{IL}



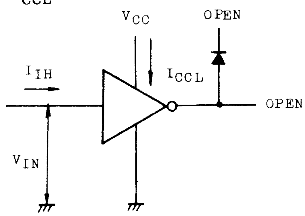
2. I_{OH}



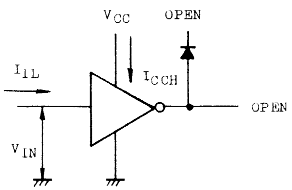
3. V_{OL}



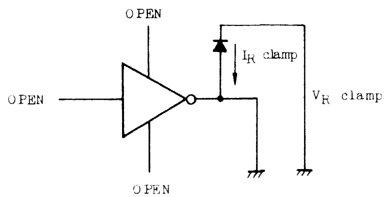
4. I_{IH}, I_{CCL}



5. I_{IL}, I_{CCH}

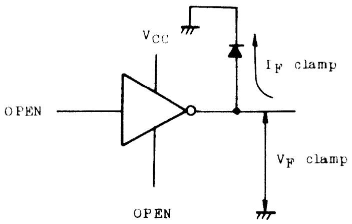


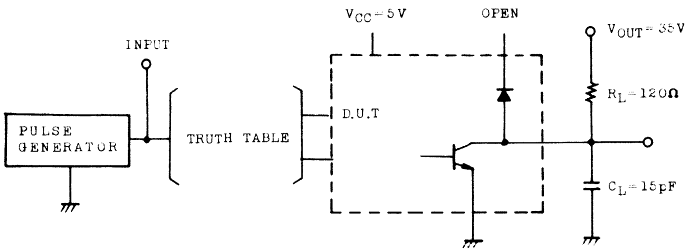
6. I_R clamp

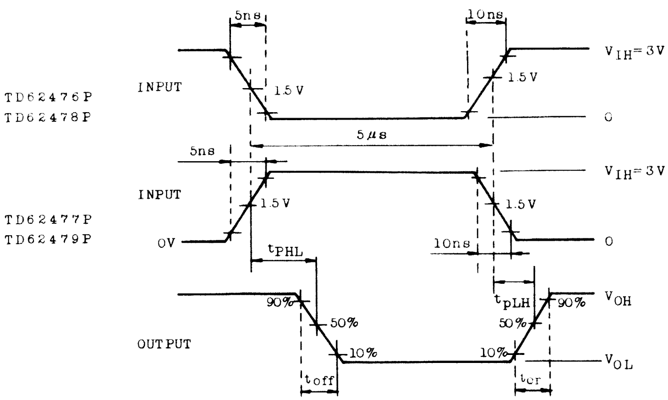


TD62476P, TD62477P
TD62478P, TD62479P

7. V_F clamp







TD62501P～TD62507P

BIPOLAR DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

SINGLE DRIVER

TD62501P COMMON EMITTER
TD62502P COMMON EMITTER
TD62503P COMMON EMITTER
TD62504P COMMON EMITTER
TD62505P COMMON COLLECTOR
TD62506P COMMON COLLECTOR
TD62507P ISOLATED

Features

- Output Current .... 200mA Max.
- High Voltage Outputs...35V
- Input Compatible with Various Types of Logic

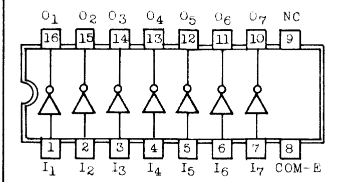
TD62501P, TD62505P, TD62507P	Using external resistor	General Purpose
TD62502P	R_{IN}=10.5kΩ + 7V Zener Diode ...	14∿25V P-MOS
TD62503P, TD62506P	R_{IN}=2.7kΩ	TTL, 5V C-MOS
TD62504P	R_{IN}=10.5kΩ	6∿15V P-MOS, C-MOS

Description

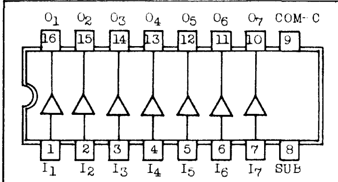
The TD62501P Series are comprised of seven or five NPN Transistor Arrays.
For proper operation, the substrate (SUB) must be connected to the most negative voltage.

PIN CONNECTIONS (TOP VIEW)

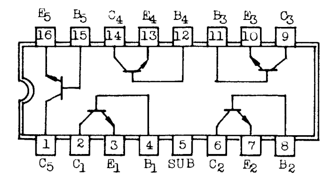
TD62501P, TD62502P, TD62503P
TD62504P



TD62505P, TD62506P



TD62507P

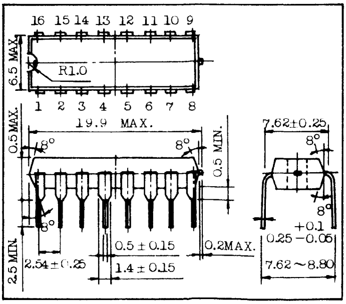


MAXIMUM RATINGS (Ta=25°C, unless otherwise noted)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Collector-Emitter Voltage	V_{CEO}	35	V
Collector-Base Voltage	V_{CBO}	50	V
Collector Current	I_C	200	mA
Input Voltage	V_{IN} *	-0.5∿+45	V
	V_{IN} **	-0.5∿+30	
Input Current	I_{IN} ***	25	mA
Isolation Voltage	V_{SUB}	35	V
GND Terminal Voltage	I_{GND}	500	mA
Power Dissipation	P_D	1.0	W
Operating Temperature	T_{opr}	-30∿+75	°C
Storage Temperature	T_{stg}	-55∿+150	°C

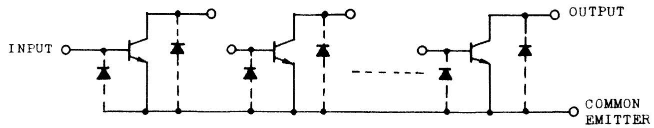
* TD62506P
** TD62502P, TC62503P, TD62504P
*** TD62501P, TD62505P, TD62507P

PACKAGE Unit: mm

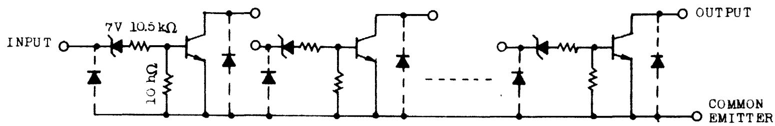


SCHEMATICS

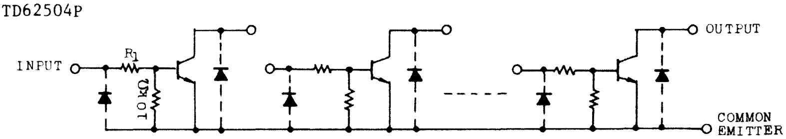
TD62501P



TD62502P

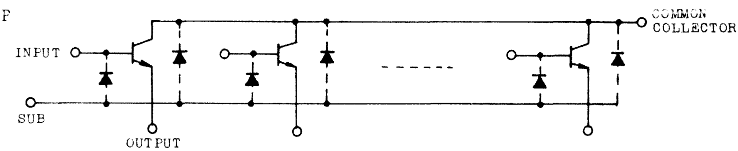


TD62503P
TD62504P

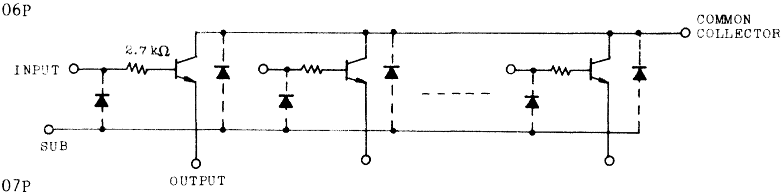


TD62503P $R_1 = 2.7\,k\Omega$, TD62504P $R_1 = 10.5\,k\Omega$

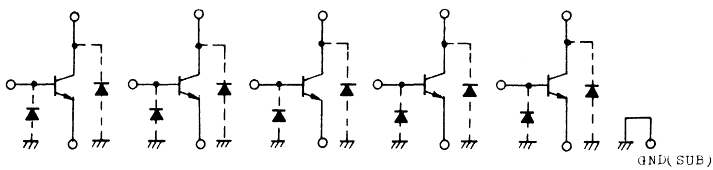
TD62505P



TD62506P



TD62507P



TD62501P～TD62507P

RECOMMENDED OPERATING CONDITIONS (Ta=-30∿+75°C)

CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Collector-Emitter Voltage		V_{CEO}		0		35	V
Collector-Base Voltage		V_{CBO}		0		50	V
Collector Current		I_C		0		150	mA
Input Voltage	TD62506P	V_{IN}		0		35	V
	TD62502P TD62503P TD62504P			0		25	
Input Current	TD62501P TD62505P TD62507P	I_{IN}		0		10	mA
Power Dissipation		P_D				0.44	W

ELECTRICAL CHARACTERISTICS (Ta=25°C)

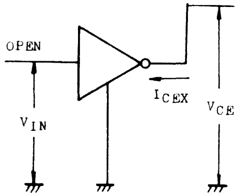
CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Output Leak Current	I_{CEX}	1	V_{CE}=25V, V_{IN}=0				10	μA
Collector - Emitter Saturation Voltage	$V_{CE}(sat)$	2	I_{IN}=1mA, I_C=10mA				0.2	V
			I_{IN}=3mA, I_C=150mA *				0.8	
DC Forward Current Transfer Ratio	h_{FE}	2	V_{CE}=10V I_C=10mA	**	70		400	
				***	50		400	
Input Voltage (Output ON)	$V_{IN}(ON)$	3	I_{IN}=1mA I_C=10mA	TD62502P	13	17	23	V
				TD62503P	2.4	3.4	4.2	
				TD62504P	7.5	11.5	15	
Turn-ON Delay	t_{ON}	4	V_{OUT}=35V, R_L=175Ω C_L=15pF			50		nS
Turn-OFF Delay	t_{OFF}					200		

* EXCEPT TD62502P

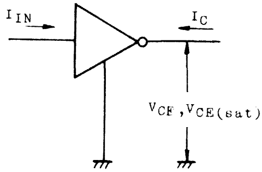
** TD62501P, TD62505P, TD62506P, TD62507P

*** TD62502P, TD62503P, TD62504P

1. I_{CEX}

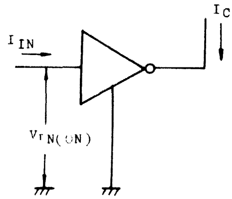


2. h_{FE}, $V_{CE}(sat)$

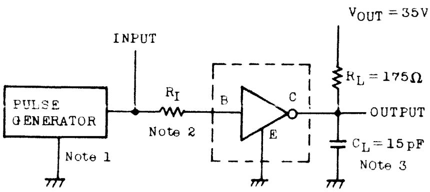


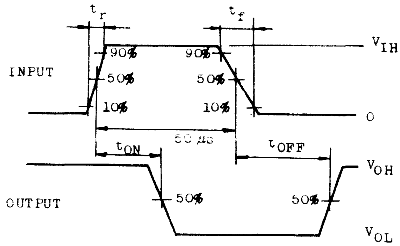
$$h_{FE} = \frac{I_C}{I_{IN}}$$

3. $V_{IN}(ON)$



4. t_{ON}, t_{OFF}





Notes: 1. Pulse Width 50μS
Duty Cycle 10%
Output Impedance 50Ω
$t_r \leq 5nS$, $t_f \leq 10nS$

3. C_L includes probe and jig capacitance.

2. See below

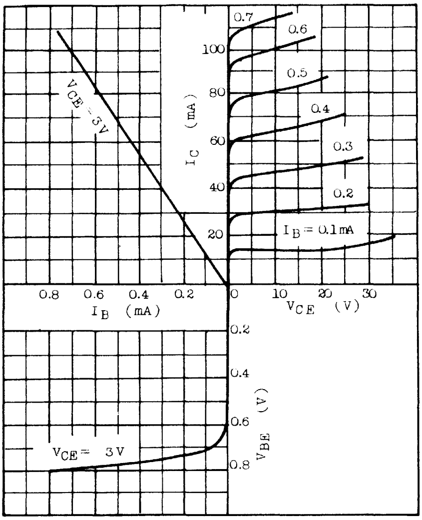
Input Conditions

Type Number	R_I	V_{IH}
TD62501P	2.7kΩ	3V
TD62502P	0	15V
TD62503P	0	3V
TD62504P	0	10V
TD62505P	2.7kΩ	3V
TD62506P	0	3V
TD62507P	2.7kΩ	3V

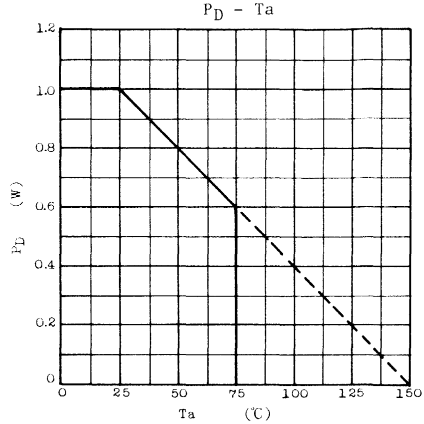
TD62501P～TD62507P

TD62501P, TD62505P, TD62507P

STATIC CHARACTERISTICS

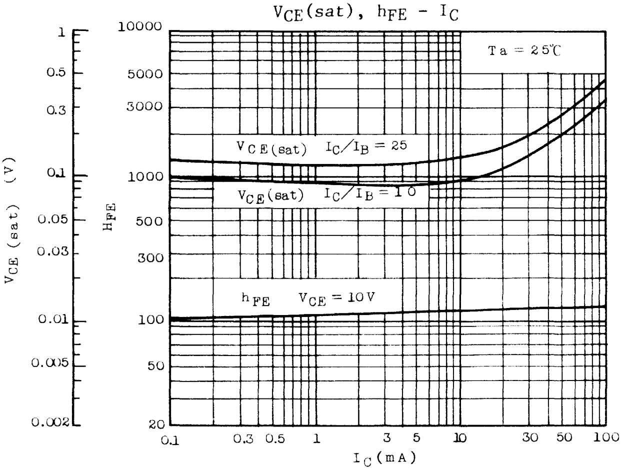


P_D - Ta



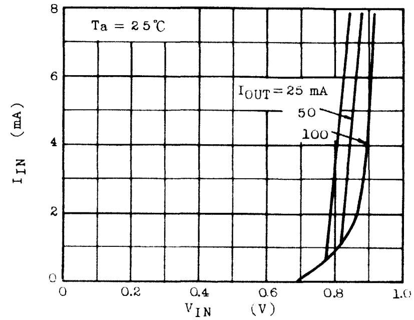
TD62501P, TD62505P, TD62507P

V_{CE}(sat), h_{FE} - I_C

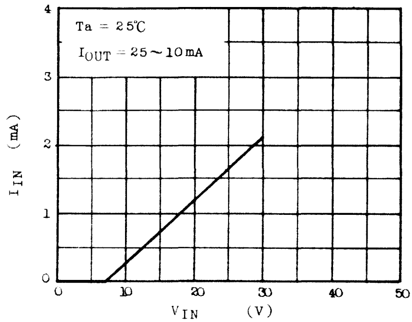


TD62501P～TD62507P

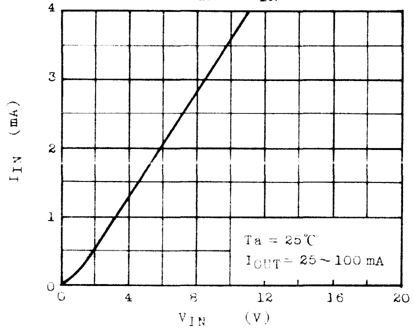
TD62501P V_{IN} - I_{IN}



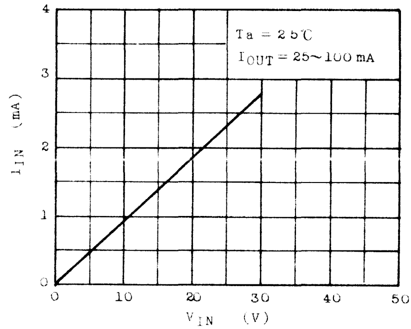
TD62502P V_{IN} - I_{IN}



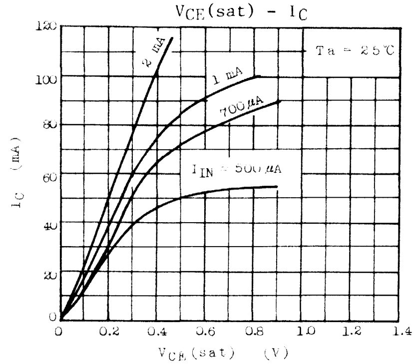
TD62503P V_{IN} - I_{IN}



TD62504P V_{IN} - I_{IN}



V_{CE}(sat) - I_C



TD62551S, TD62553S TD62554S, TD62555S

BIPOLAR DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

SINGLE DRIVER
TD62551S COMMON EMITTER
TD62553S COMMON EMITTER
TD62554S COMMON EMITTER
TD62555S COMMON EMITTER

Features

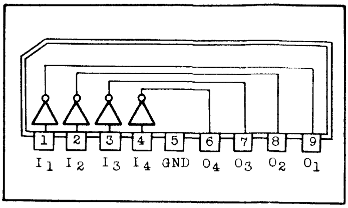
- Output Current .... 150 mA Max.
- High Voltage Output 25V
- Input Compatible with Various Types of Logic

TD62551S
Using external resistor ... General Purpose
TD62553S R_{IN}=2.7kΩ .... TTL. 5VCMOS
TD62554S R_{IN}=10.5kΩ .... 6∿15V P-MOS, C-MOS
TD62555S R_{IN}=20kΩ .... 14∿20V P-MOS

Description

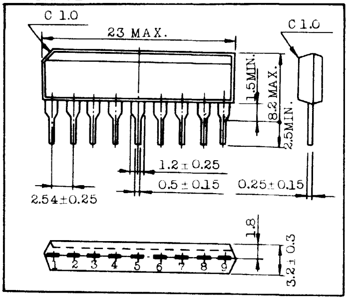
The TD62551S Series are comprised of four NPN Transistor Arrays.
These devices are specifically designed for LED and lamp drive.

PIN CONNECTION



PACKAGE

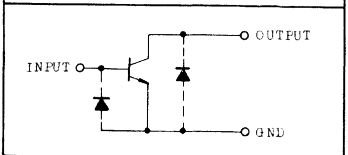
Unit: mm



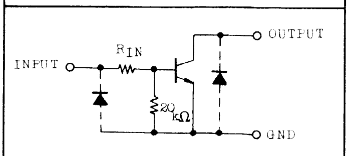
SCHEMATICS

(EACH DRIVER)

TD62551S



TD62553S, TD62554S
TD62555S



TD62553S R_{IN} = 2.7kΩ
TD62554S R_{IN} = 10.5 kΩ
TD62555S R_{IN} = 20 kΩ

MAXIMUM RATINGS (Ta=25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Collector-Emitter Voltage	V_{CEO}	25	V
Collector-Base Voltage	V_{CBO}	35	V
Collector Current	I_C	150	mA
Input Voltage	V_{IN} *	20	V
Input Current	I_{IN} **	10	mA
GND Terminal Voltage	I_{GND}	400	mA
Power Dissipation	P_D	0.75	W
Operating Temperature	T_{opr}	-30 ∿ +75	°C
Storage Temperature	T_{stg}	-55 ∿ +150	°C

* Except TD62551S
** Only TD62551S

TD62551S, TD62553S
TD62554S, TD62555S

RECOMMENDED OPERATING CONDITIONS (Ta=-30 ∿ +75°C)

CHARACTERISTIC	SYMBOL	CONDITION		MIN.	TYP.	MAX.	UNIT
Collector-Emitter Voltage	V_{CEO}			0		25	V
Collector-Base Voltage	V_{CBO}			0		35	V
Collector Current	I_C	TD62551S, TD62553S		0		100	mA
		TD62554S		0		80	mA
		TD62555S		0		60	mA
Input Voltage	V_{IN}		TD62553S	0		20	V
			TD62554S	0		20	V
			TD62555S	0		20	V
Input Current	I_{IN}		TD62551S	0		5	mA
Power Dissipation	P_D					0.33	W

ELECTRICAL CHARACTERISTICS (Ta=25°C)

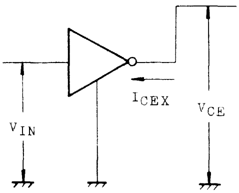
CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Output Leak Current	I_{CEX}	1	V_{CE}=25V, V_{IN}=0				10	μA
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	2	I_{IN}=0.5mA, I_C=10mA			0.15	0.2	V
			I_{IN}=2.5mA, I_C=50mA			0.35	0.5	V
DC Forward Current Transfer Ratio	h_{FE}	2	V_{CE}=5V, I_C=10mA	*	60		400	
				**	50		400	
Input Voltage (Output ON)	$V_{IN(ON)}$	3	I_{IN}=0.5mA, I_C=10mA	TD62553S	1.7	2.1	2.5	V
				TD62554S	4.4	6.0	7.6	V
				TD62555S	7.7	10.7	13.8	V
Turn-ON Delay	t_{ON}	4	V_{OUT}=25V, R_L=500Ω, C_L=15pF			100		nS
Turn-OFF Delay	t_{OFF}	4				500		nS

* Only TD62551S
** Except TD62551S

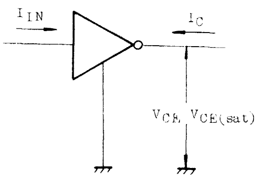
TD62551S, TD62553S
TD62554S, TD62555S

TEST CIRCUIT

1. I_{CEX}

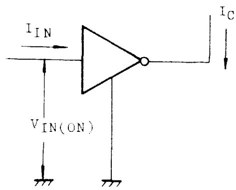


2. h_{FE}, $V_{CE(sat)}$

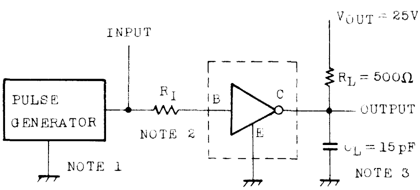


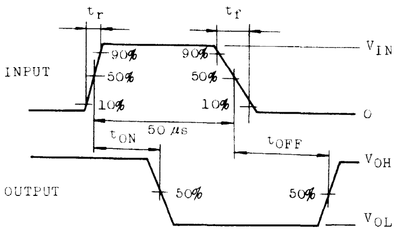
$$h_{FE} = \frac{I_C}{I_{IN}}$$

3. $V_{IN(ON)}$



4. t_{ON}, t_{OFF}





Notes: 1. Pulse Width 50μs
Duty Cycle 10%
Output Impedance 50Ω
$t_r \leqq 5$ ns, $t_f \leqq 10$ ns

3. C_L includes probe and jig capacitance

2. See below
Input Conditions

Type number	R_I	V_{IH}
TD62551S	2.7kΩ	3V
TD62553S	0	3V
TD62554S	0	10V
TD62555S	0	14V

BIPOLAR DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TD62601P, TD62602P
TD62603P, TD62604P

HEX THRESHOLD FREE DRIVER

TD62601P INVERTER
TD62602P INVERTER/OPEN COLLECTOR
TD62603P NON-INVERTER
TD62604P NON-INVERTER/OPEN COLLECTOR

Features

- Wide Supply Voltage Range V_{CC}=4 ∿ 18V
- Vref=1/2 V_{CC} #16 PIN is Non-Connected
- Pin Compatible with C-MOS LOGIC 4049B, 4050B type.

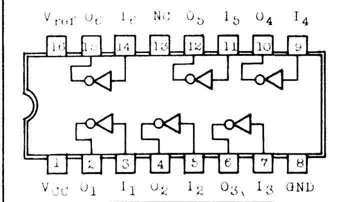
TD62601P (4049B type)
TD62602P (4049B type Open-Collector)
TD62603P (4050B type)
TD62604P (4050B type Open-Collector)

Description

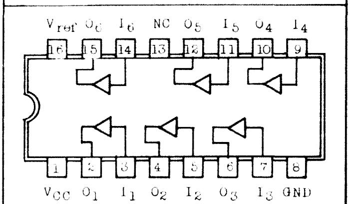
The TD62601P Series are threshold free drivers which are comprised of six NPN transistor output stages and comparator input stages. The TD62601P Series are pin compatible with C-MOS 4049B and 4050B type except V_{ref} terminal. V_{ref} is set at 1/2 Vcc with internal resistors and it is changeable using external resistors.

PIN CONNECTIONS (TOP VIEW)

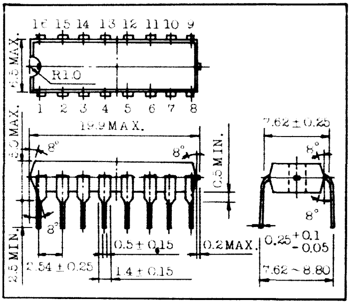
TD62601P, TD62603P



TD62603P, TD62604P



PACKAGE Unit: mm

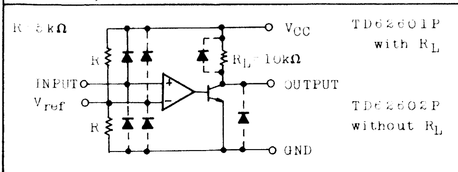


MAXIMUM RATINGS (Ta=25°C, unless otherwise noted)

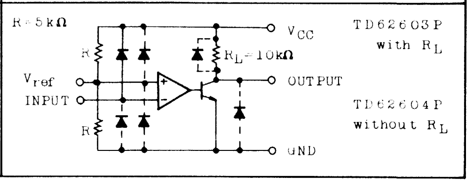
CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	20	V
Output Voltage	V_{OUT}	-0.5 ∿ +20	V
Output Current	I_{OUT}	10	mA
Input Voltage	V_{IN}	-0.5 ∿ V_{CC} + 0.5	V
Power Dissipation	P_D	1.0	W
Operating Temperature	T_{opr}	-40 ∿ +85	°C
Storage Temperature	T_{stg}	-55 ∿ +150	°C

SCHEMATICS (EACH DRIVER)

TD62601P, TD62602P



TD62603P, TD62604P



TD62601P, TD62602P
TD62603P, TD62604P

RECOMMENDED OPERATING CONDITIONS (Ta=-40 ∿ +85°C)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}		4.0		18	V
Output Voltage	V_{OUT}	TD62602P, TD62604P	0		18	V
Output Current	I_{OUT}	V_{CC}=5V	0		8	mA
Input Voltage	V_{IN}		0		V_{CC}	V
V_{ref} Input Voltage	Vref	Ta=25°C	0.4		V_{CC} -1.6	V
Power Dissipation	P_D				0.36	W

ELECTRICAL CHARACTERISTICS (Ta=25°C)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
"H" Level Input Voltage		V_{IH}			V_{ref} +0.1			V
"L" Level Input Voltage		V_{IL}					V_{ref} -0.1	V
"H" Level Output Current	TD62602P TD62604P	I_{OH}		V_{CC}=4.5V V_O=18V			10	μA
"H" Level Output Voltage	TD62601P TD62603P	V_{OH}		V_{CC}=4.5V I_O=-10μA	4.3			V
"L" Level Output Voltage		V_{OL}		V_{CC}=4.5V, I_O=8mA		0.1	0.4	V
"H" Level Input Current		I_{IH}		V_{CC}=18V, V_{IN}=18V			2	μA
"L" Level Input Current		I_{IL}		V_{CC}=18V, V_{IN}=0V		-0.2	-1.5	μA
V_{ref} Terminal Voltage		$V_{ref(OUT)}$			$\frac{1}{2}V_{CC}$ -0.1		$\frac{1}{2}V_{CC}$ +0.1	V
V_{ref} Resistor		R			3.5	5	6.5	kΩ
Supply Current		I_{CC}					12	mA
		I_{CCL}		TD62601P, TD62603P			27	
Turn-ON Delay		t_{ON}						μS
Turn-OFF Delay		t_{OFF}						μS

BIPOLAR DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TD62703P

TD62703P HIGH VOLTAGE SOURCE CURRENT DRIVER

Features

- High Output Voltage $V_{CC}-V_{OUT}$=60V Min.
- Output Current I_{OUT}=-50mA Max.
- Input Resistor R_{IN}=2.7kΩ

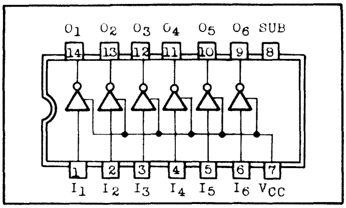
Description

The TD62703P is comprised of six source current drivers.

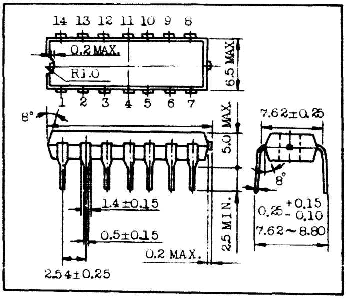
This driver is specifically designed for fluorescent display applications.

For proper operation, the substrate (SUB) must be connected to the most negative voltage.

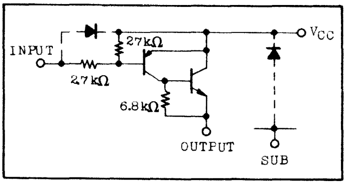
PIN CONNECTION



PACKAGE



SCHEMATIC



MAXIMUM RATINGS (Ta=25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{SUB}	V_{CC}-60	V
Output Voltage	V_{OUT}	V_{CC}-60	V
Input Voltage	V_{IN}	-30 ∿ +0.5	V
Output Current	I_{OUT}	-50	mA
Input Current	I_{IN}	10	mA
Power Dissipation	P_D	1.0	W
Operating Temperature	T_{opr}	-30 ∿ +75	°C
Storage Temperature	T_{stg}	-55 ∿ +150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=-30 ∿ +75°C)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{SUB}	V_{CC}= 0V	V_{OUT}		-55	V
Output Voltage	V_{OUT}		0		V_{SUB}	V
Output Current	I_{OUT}		0		-40	mA
Input Voltage	V_{IN}		0		-7.0	V
Power Dissipation	P_D				0.44	W

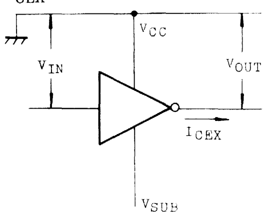
TD62703P

ELECTRICAL CHARACTERISTICS (Ta=25°C)

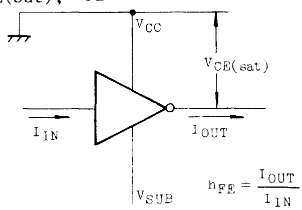
CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Leak Current		I_{CEX}	1	V_{CC}=0V, V_{IN}=0V, V_{OUT}=-55V			-100	μA
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$	2	I_{IN}=-1mA, I_{OUT}=-40mA			-2.5	V
DC Forward Current Transfer Ratio		h_{FE}	2	V_{CE}=-5.0V, I_{OUT}=-40mA	100			
Input Current	Output ON	$I_{IN(ON)}$	3	V_{CC}=0V, V_{IN}=-5.1V		-1.7	-2.4	mA
	Output OFF	$I_{IN(OFF)}$	3				10	μA
Input Voltage	Output ON	$V_{IN(ON)}$	4	V_{CC}=0V	-3.0			V
	Output OFF	$V_{IN(OFF)}$	4	V_{CC}=0V			-0.44	V
Turn-ON Delay		t_{ON}	5	V_{CC}=0V, V_{SUB}=V_{OUT}=-55V			1	μs
Turn-OFF Delay		t_{OFF}		R_L=1.4kΩ, C_L=15pF			2	

TEST CIRCUIT

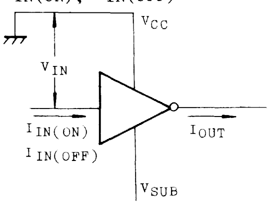
1. I_{CEX}



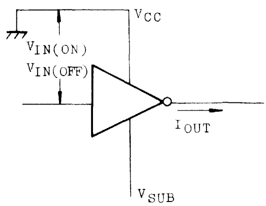
2. $V_{CE(sat)}$, h_{FE}



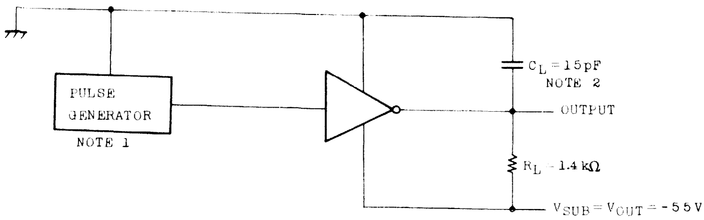
3. $I_{IN(ON)}$, $I_{IN(OFF)}$

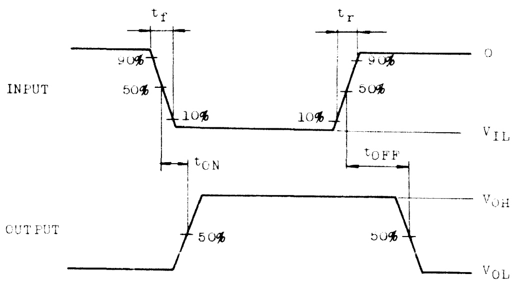


4. $V_{IN(ON)}$, $V_{IN(OFF)}$



5. t_{ON}, t_{OFF}

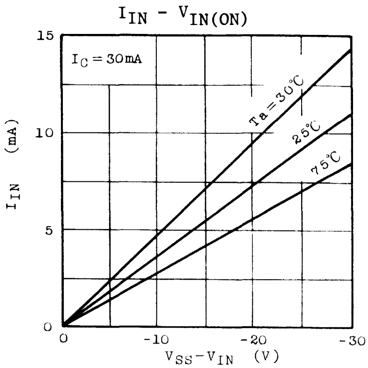


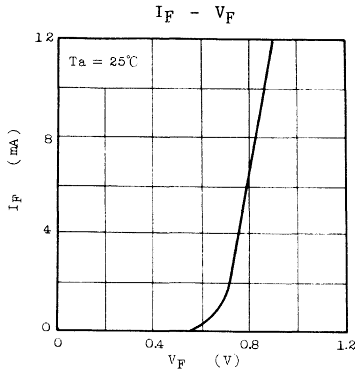


Notes: 1. Pulse Width = 50μS
Duty Cycle = 10%
Output Impedance = 50Ω
$t_r \leqq 10$ ns
$t_f \leqq 5$ ns

2. C_L includes probe and jig capacitance

TD62703P


I_{IN} - $V_{IN(ON)}$
$I_C = 30mA$
Ta = 30°C
25°C
75°C
I_{IN} (mA)
15
10
5
0
0
-10
-20
-30
$V_{SS}-V_{IN}$ (V)


I_F - V_F
Ta = 25°C
I_F (mA)
12
8
4
0
0
0.4
0.8
1.2
V_F (V)

BIPOLAR DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TD62705P, TD62706P

TD62705P HIGH VOLTAGE SOURCE CURRENT DRIVER
TD62706P HIGH VOLTAGE SOURCE CURRENT DRIVER

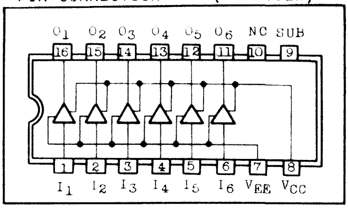
Features

- High Output Voltage $V_{CC}-V_{OUT}=60V$ Min.
- Output Current $I_{OUT}=-50mA$ Max
- Input Compatible with Various Types of Logic.
  TD62705P $R_{IN}=47k\Omega$ 6 ∿ 25V P-MOS, C-MOS
  TD62706P $R_{IN}=10k\Omega$ TTL. 5V C-MOS

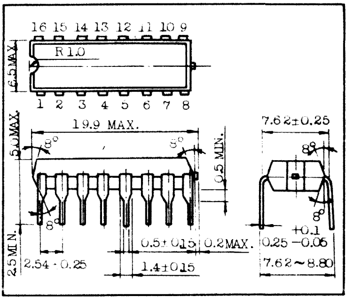
Description

The TD62705P and TD62706P are comprised of six source current drivers.
These drivers are specifically designed for fluorescent display applications.
For proper operation the substrate (SUB) must be connected to the most negative voltage.

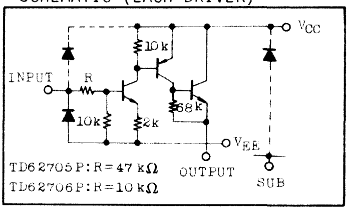
PIN CONNECTION (TOP VIEW)



PACKAGE unit: mm



SCHEMATIC (EACH DRIVER)



MAXIMUM RATINGS (Ta=25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	$V_{CC}-V_{EE}$	30	V
	$V_{CC}-V_{SUB}$	60	V
Output Voltage	$V_{CC}-V_{OUT}$	60	V
Input Voltage	$V_{IN}-V_{EE}$	$V_{CC}-V_{EE}$	V
Output Current	I_{OUT}	-50	mA
Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	1.0	W
Operating Temperature	T_{opr}	-30 ∿ +75	°C
Storage Temperature	T_{stg}	-55 ∿ +150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=-30 ∿ +75°C)

CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	TD62705P	V_{CC}	V_{EE} = 0V	6.0		25	V
	TD62706P			4.5		25	
		V_{SUB}	V_{CC} = 0V	V_{OUT}		-55	V
Output Voltage		V_{OUT}	V_{CC} = 0V	0		-55	V
Output Current		I_{OUT}		0		-40	mA
Input Voltage	TD62705P	V_{IN}	V_{EE}=0V, V_{CC}=25V	0		25	V
	TD62706P			0		7	
Power Dissipation		P_D				0.44	W

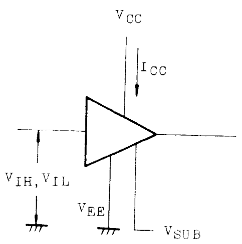
TD62705P, TD62706P

ELECTRICAL CHARACTERISTICS (Ta=25°C)

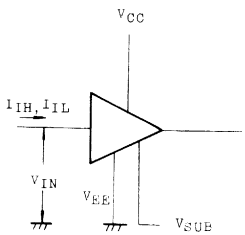
CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
"H" Level Input Voltage	TD62705P	V_{IH}	1	V_{EE}=0V	6.0	–	–	V
	TD62706P			V_{EE}=0V	2.2	–	–	
"L" Level Input Voltage	TD62705P	V_{IL}	1	V_{EE}=0V	–	–	2.2	V
	TD62706P			V_{EE}=0V			0.8	
"H" Level Input Current	TD62705P	I_{IH}	2	V_{EE}=0V, V_{IN}=6.0V		0.11	0.16	mA
	TD62706P			V_{EE}=0V, V_{IN}=2.4V		0.12	0.18	
"L" Level Input Current		I_{IL}	2	V_{EE}=V_{IN}=0V, V_{CC}=25V	–	–	±1	μA
Output Leak Current		I_{CEX}	3	V_{EE}=0V, V_{CC}=25V V_{IN}=V_{IL} max, V_{OUT}=-30V	–	–	-100	μA
Collector - Emitter Saturation Voltage		$V_{CE(sat)}$	4	V_{EE}=0V, V_{CC}=V_{CC} min. V_{IN}=V_{IH} min, I_{OUT}=-40mA			V_{CC}-2.5	V
Supply Current	TD62705P	I_{CC}	1	V_{EE}=0V, V_{CC}=25V V_{IN}=V_{IN} max, I_{OUT}=0mA			32	mA
	TD62706P						25	
Turn-ON Delay		t_{ON}	5	R_L=1.4kΩ, C_L=15pF	–	0.2	–	μs
Turn-OFF Delay		t_{OFF}			–	1.5	–	

TEST CIRCUIT

1. V_{IH}, V_{IL}, I_{CC}

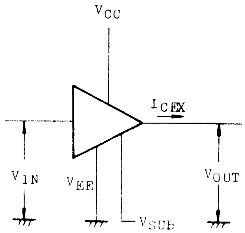


2. I_{IH}, I_{IL}

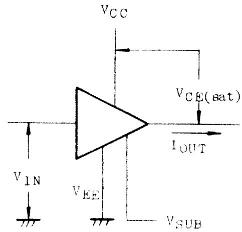


TD62705P, TD62706P

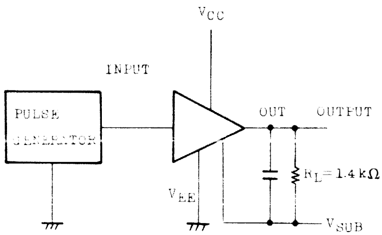
3. I_{CEX}



4. $V_{CE(sat)}$



5.

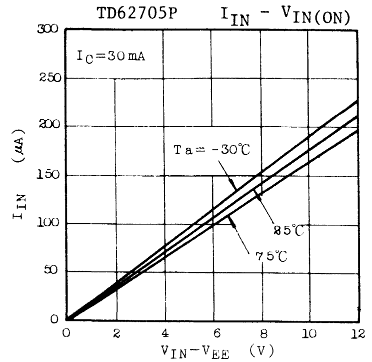


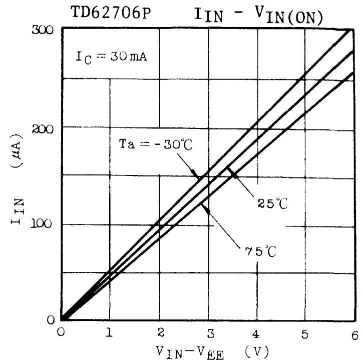
Input conditions

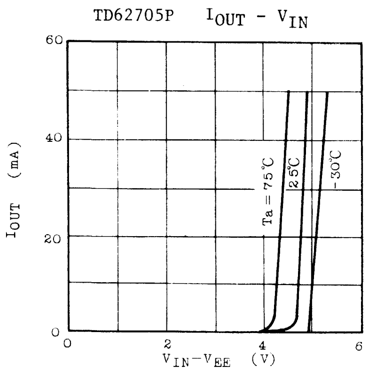
Type	V_{IN}	V_{CC}	V_{SUB}
TD62705P	0–9V	25V	-30
TD62706P	0–3V	25V	-30

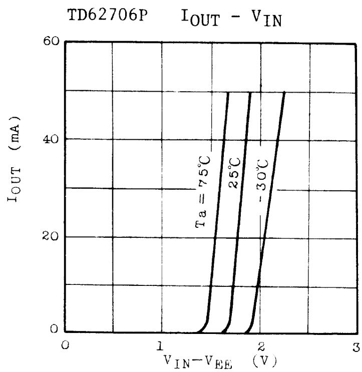
V_{IN}: Pulse Width = 50μs
Duty Cycle = 50%
$t_r \leqq 5$ ns
$t_f \leqq 10$ ns

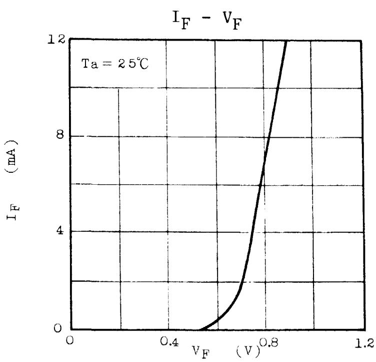
TD62705P, TD62706P

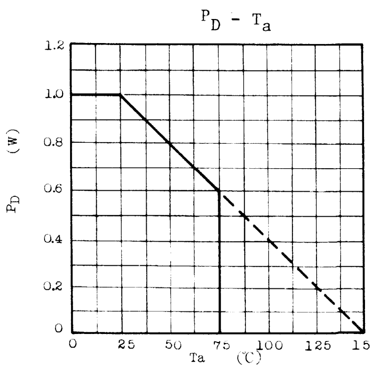












BIPOLAR DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TD62781AP, TD62782AP

TENTATIVE

TD62781AP HIGH CURRENT SOURCE DRIVER
TD62782AP HIGH CURRENT SOURCE DRIVER

Features

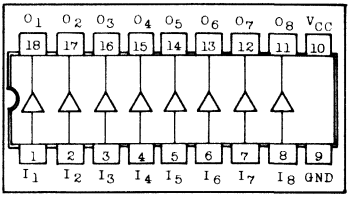
- High Output Voltage..........V_{CC}=60V
- Output Current...............I_{OUT}=50mA Max.
- Pull-Down Registers/Each Output
- Single Supply Voltage
- Inputs Compatible with Various Types of Logic

TYPE	DESIGNATION
TD62781AP	TTL, 5V C-MOS
TD62782AP	6 ~ 15V P-MOS, C-MOS

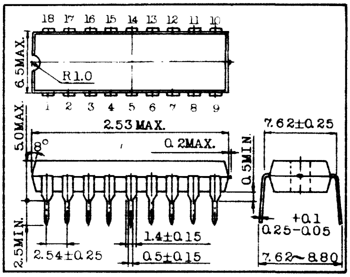
Description

The TD62781AP and TD62782AP are comprised of eight source current drivers.
These drivers are specifically designed for fluorescent display applications.

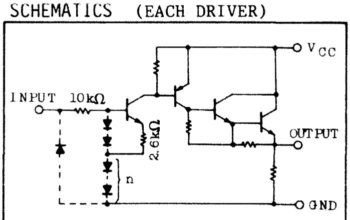
PIN CONNECTION (TOP VIEW)



PACKAGE Unit: mm



SCHEMATICS (EACH DRIVER)



TD62781AP : n=1, TD62782AP : n=4

MAXIMUM RATINGS (Ta=25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	60	V
Output Voltage	V_{OUT}	V_{CC}	V
Output Current	I_{OUT}	-50	mA
Input Voltage	V_{IN}	20	V
GND Terminal Current	I_{GND}	1	A
Power Dissipation	P_D	1.47	W
Operating Temperature	T_{opr}	-40~ +85	°C
Storage Temperature	T_{stg}	-55 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=-40 ~ +85°C)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	TD62781AP	V_{CC}		4.5		55	V
	TD62782AP			6.0		55	
Output Voltage		V_{OUT}		0		V_{CC}	V
Output Current		I_{OUT}		0		-40	mA
Input Voltage	TD62781AP	V_{IN}		0		7	V
	TD62782AP			0		15	
Power Dissipation		P_D				0.52	W

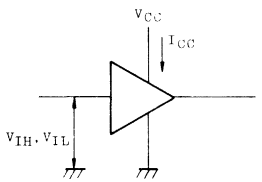
TD62781AP, TD62782AP

ELECTRICAL CHARACTERISTICS (Ta=25°C)

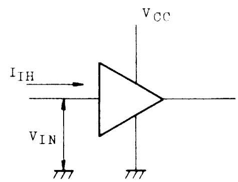
CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
"H" Level Input Voltage	TD62781AP	V_{IH}	1		2.0			V
	TD62782AP				4.0			
"L" Level Input Voltage	TD62781AP	V_{IL}	1				0.8	V
	TD62782AP						2.0	
"H" Level Input Current	TD62781AP	I_{IH}	2	V_{IN}=2.4V		36	55	μA
	TD62782AP			V_{IN}=7.5V		340	500	
"L" Level Output Current		I_{OL}	3					μA
"H" Level Output Voltage		V_{OH}	4	I_{OUT}=-40mA, V_{IN}=V_{IH} Min.	V_{CC} -2.5	V_{CC} -1.7		V
"L" Level Output Voltage		V_{OL}		I_{OUT}=0, V_{IN}=V_{IL} Max.		50	250	mV
Supply Current		$I_{CC(ON)}$	1	V_{CC}=55V, V_{IN}=V_{IH} Min.				
		$I_{CC(OFF)}$		V_{CC}=55V, V_{IN}=V_{IL} Max.				
Turn-ON Delay		t_{ON}						μs
Turn-OFF Delay		t_{OFF}						

TEST CIRCUIT

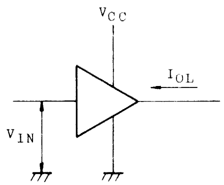
1. V_{IH},V_{IL}, I_{CC}



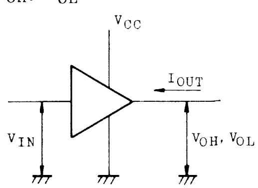
2. I_{IH}



3. I_{OL}



4. V_{OH}, V_{OL}



BIPOLAR DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TD62801P

TD62801P
8 BIT SHIFT REGISTER/LATCH/DRIVER
(THERMAL HEAD DRIVER)

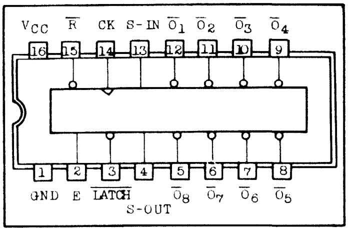
Features

- 8 Bit Serial-In Parallel-Out Shift Register/Latch/ 8 Bit Driver Transistors.
- Output Current .... 70 mA Max.
- High Output Voltage .... 26 V
- TTL Compatible Inputs
- Internal Auto Reset Function
- Standard Supply Voltage

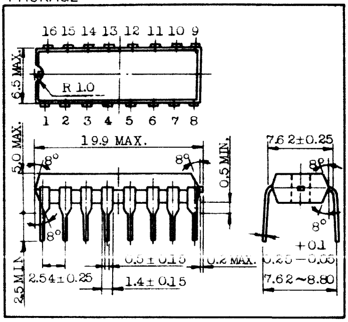
Description

The TD62801P is specifically designed for thermal printing head drivers utilizing a new high speed, high voltage I^2L process.

PIN CONNECTION (TOP VIEW)



PACKAGE Unit: mm



MAXIMUM RATINGS (Ta=0 ∿ 70°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	-0.3 ∿ +6.0	V
Input Voltage	V_{IN}	-0.3 ∿ V_{CC}+0.3	V
Output Voltage	V_{OUT} *	-0.3 ∿ V_{CC}+0.3	V
Output Sustaining Voltage	$V_{CE(SUS)}$**	-0.3 ∿ +26	V
Input Current	I_{IN}	±1	mA
Output Current	I_{OUT} **	70	mA
Power Dissipation	P_D	0.8	W
Operating Temperature	T_{opr}	0 ∿ +70	°C
Storage Temperature	T_{stg}	-55 ∿ +150	°C

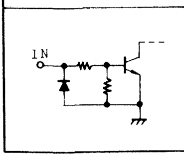
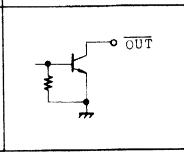
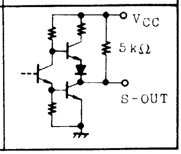
* S-OUT ** $\overline{O_1}$ ∿ $\overline{O_8}$

TRUTH TABLE

CK	E	$\overline{R}$	$\overline{LATCH}$	S-IN	OUT $\overline{O1}$	OUT $\overline{On}$	S-OUT
↑	H	H	H	L	OFF	$\overline{On-1}$	O7
↑	H	H	H	H	ON	$\overline{On-1}$	O7
↑	H	H	L	*	NC	NC	O7
↑	L	H	*	*	NC	NC	O7
↓	*	*	*	*	NC	NC	O7
*	*	L	H	*	OFF	OFF	L
*	H	⊔	L	*	NC	NC	L

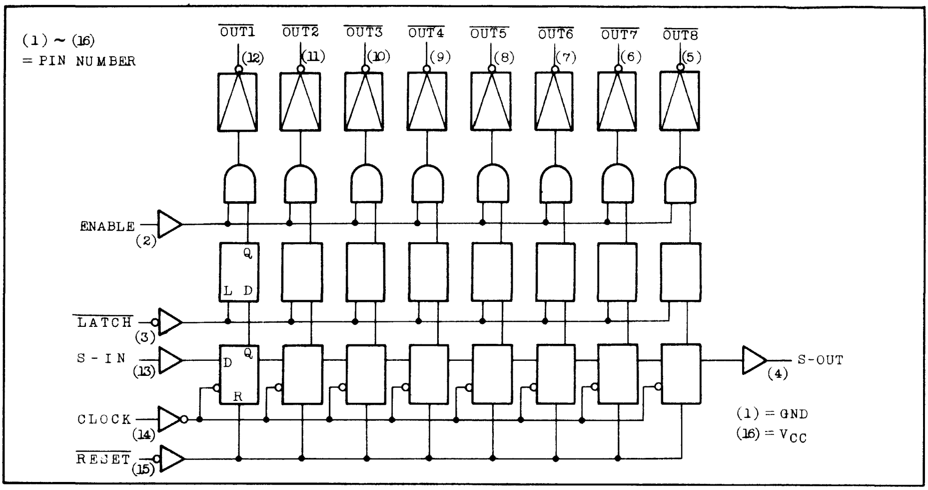
CK=CLOCK *=DON'T CARE
E=ENABLE NC=NO CHANGE
$\overline{R}$=RESET L=LOW LEVEL
$\overline{LATCH}$=LATCH H=HIGH LEVEL
S-IN=SERIAL IN
OUT=PARALLEL OUT
S-OUT=SERIAL OUT

EQUIVALENT OF INPUTS AND OUTPUTS

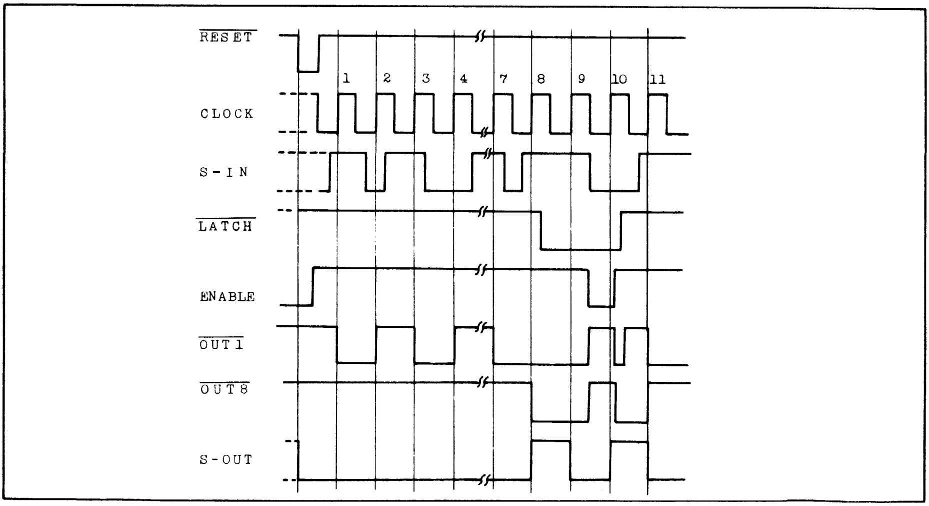
INPUT	$\overline{O_1}$ ∿ $\overline{O_8}$	S-OUT
		

TD62801P

BLOCK DIAGRAM



TIMING DIAGRAM



RECOMMENDED OPERATING CONDITIONS (Ta=0 ∿ 70°C)

CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage		V_{CC}		4.5	5.0	5.5	V
Input Voltage		V_{IN}		0		V_{CC}	V
"H" Level Output Current	S-OUT	I_{OH}		0		-0.4	mA
"H" Level Output Voltage	$\overline{On}$	V_{OH}		0		24	V
"L" Level Output Current	S-OUT	I_{OL}		0		8	mA
	$\overline{On}$	I_{OL}		0		60	mA
Clock Frequency		f_{clock}		0		500	kHz
Clock Pulse Width		t_{w} clock		1			μs
Data Set Up Time		t_{setup}		100			ns
Data Hold Time		t_{hold}		100			ns

ELECTRICAL CHARACTERISTICS (Ta=0 ∿ 70°C)

CHARACTERISTIC		SYMBOL	CONDITION		MIN.	TYP.	MAX.	UNIT
"H" Level Input Voltage		V_{IH}			2.0			V
"L" Level Input Voltage		V_{IL}					0.8	V
"H" Level Input Current		I_{IH}	V_{CC}=5.5V	V_{IH}=2.4V		0.14	0.3	mA
				V_{IH}=5.5V		0.37	0.7	
"L" Level Input Current		I_{IL}	V_{CC}=5.5V, V_{IL}=0.4V			20	50	μA
"H" Level Output Voltage	S·OUT	V_{OH}	V_{CC}=5.0V, I_{OH}=-10μA		4.0			V
			V_{CC}=4.5V, I_{OH}=-400μA		2.4	2.8		
"H" Level Output Current	$\overline{On}$	I_{OH}	V_{CC}=4.5V, V_{OH}=24V				100	μA
"L" Level Output Voltage	S·OUT	V_{OL}	V_{CC}=4.5V, I_{OL}=8mA			0.2	0.4	V
"L" Level Output Voltage	$\overline{On}$	V_{OL}	V_{CC}=4.5V, I_{OL}=60mA			0.2	0.6	V
Short - Circuit Output Current	S·OUT	I_{OS}	V_{CC}=5.5V		-5	-16	-50	mA
Supply Current		I_{CC}	V_{CC}=5.5V			55	80	mA

TD62801P

SWITCHING CHARACTERISTICS (Ta=25°C)

CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time Low-to-High	CK-S•OUT	t_{pLH}	V_{CC}=5.0V, V_{IN}=3.0V V_{IL}=0V, Duty=50% R_L S•OUT=2kΩ R_L $\overline{\text{On}}$=82Ω C_L=15pF		0.6	1.5	μs
	CK-$\overline{\text{On}}$				2.5	6.5	
	$\overline{\text{L}}$-$\overline{\text{On}}$				2.1	5.0	
	$\overline{\text{R}}$-$\overline{\text{On}}$				2.2	6.0	
	E-$\overline{\text{On}}$				1.5	4.0	
Propagation Delay Time High-to-Low	CK-S•OUT	t_{pHL}			0.35	1.0	μs
	CK-$\overline{\text{On}}$				0.6	1.5	
	$\overline{\text{L}}$-$\overline{\text{On}}$				0.32	1.0	
	$\overline{\text{R}}$-S•OUT				0.3	1.0	
	E-$\overline{\text{On}}$				0.1	0.3	
Maximum Clock Frequency		f_{max}			1.6		MHz
Minimum Clock Pulse Width	CK	t_{WCK}			250	600	ns
		$\overline{t_{WCK}}$			280	700	
	L	t_{WL}			230	600	
	$\overline{\text{R}}$	t_{WR}			300	1000	
Set Up Time		t_{setup}			20	50	ns
Hold Time		t_{hold}			20	50	ns
Rise Time		t_r			70		ns
Fall Time		t_f			70		ns

BIPOLAR DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

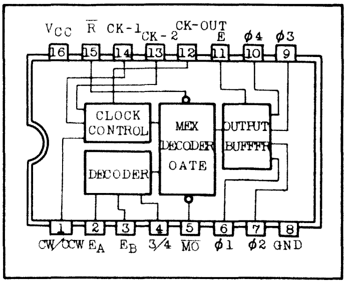
TD62803P

TD62803P STEPPING MOTOR CONTROLLER/DRIVER

Features

- High-Voltage, High-Current Outputs
  $V_{CE}(SUS)\phi$=28V(MIN), $I_{OUT}\phi$=400mA (MAX)
- 1,2, 1-2 Phase Excitation Mode Capable
- 3 Inputs Direction Control .. CK-1, CK-2 CW/CCW
- Output Enable Function ... E
- Initialized Status ..... $\overline{Mo}$ (Monitor out)
- Schmitt Trigger Inputs .... CK-1, CK-2, CW/CCW, $\overline{R}$
- Standard Supply Voltage

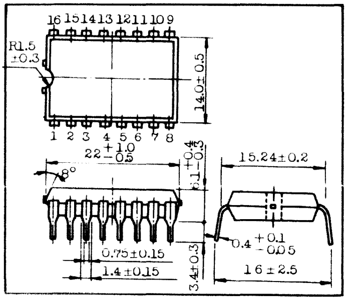
PIN CONNECTION (TOP VIEW)



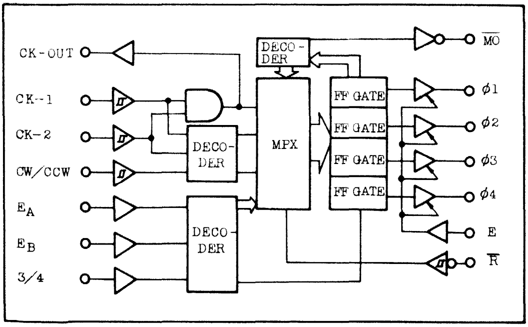
MAXIMUM RATINGS (Ta=25°C unless otherwise noted)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Supply Voltage		V_{CC}	-0.3 ∿ +7.0	V
Output Sustaining Voltage		$V_{CE}(SUS)\phi$	-0.3 ∿ +28	V
Output Current	ϕ_n	$I_{OUT}\phi$	400	mA
	$\overline{Mo}$, CK-OUT	I_{OUT} $\overline{Mo}$ CK-OUT	10	mA
Input Voltage		V_{IN}	-0.3 ∿ V_{CC}+0.3	V
Input Current		I_{IN}	±1	mA
Power Dissipation		P_D	2.7	W
Operating Temperature		T_{opr}	-30 ∿ +85	°C
Storage Temperature		T_{stg}	-55 ∿ +150	°C

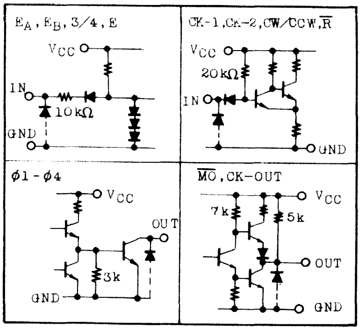
PACKAGE Unit: mm



BLOCK DIAGRAM



SCHEMATICS OF INPUTS AND OUTPUTS



TD62803P

RECOMMENDED OPERATING CONDITIONS (Ta=-30 ∿ +85°C)

CHARACTERISTIC		SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Supply Voltage		V_{CC}		4.5	5.0	5.5	V
Output Sustaining Voltage		$V_{CE(SUS)}$		0		26	V
"L" Level Output Current ϕn		$I_{OUT\phi}$				400	mA
			Test Mode			250	mA
Output Current Mo, CK-OUT	"H" Level	I_{OH}				-0.4	mA
	"L" Level	I_{OL}				8	mA
Input Voltage		V_{IN}		0		V_{CC}	V
Clock Frequency		f_{CK}		0		100	kHz
Power Dissipation		P_D				1.0	W

ELECTRICAL CHARACTERISTICS (Ta=25°C)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
"H" Level Input Voltage		V_{IH}		2.0			V
"L" Level Input Voltage		V_{IL}				0.8	V
"H" Level Output Current ϕn		$I_{OH\phi}$	V_{CC}=5.5V, V_{OUT}=26V			100	μA
"H" Level Output Voltage $\overline{Mo}$, CK-OUT		V_{OH}	V_{CC}=4.5V, I_{OH}=-0.4mA	2.4			V
			V_{CC}=5.0V I_{OH}=-10μA	4.0			V
"L" Level Output Voltage	$\overline{Mo}$, CK-OUT	V_{OL}	V_{CC}=4.5V, I_{OL}=8mA			0.4	V
	ϕn	$V_{OUT\phi}$	V_{CC}=4.5V, I_{OUT}=400mA			1.1	V
			V_{CC}=4.5V, I_{OUT}=200mA			0.6	V
"H" Level Input Current		I_{IH}	V_{CC}=5.5V, V_{IH}=5.5V			10	μA
"L" Level Input Current		I_{IL}	V_{CC}=5.5V, V_{IL}=0.4V			-0.4	mA
Hysteresis		ΔV_T		200			mV
Supply Current		I_{CC}				100	mA

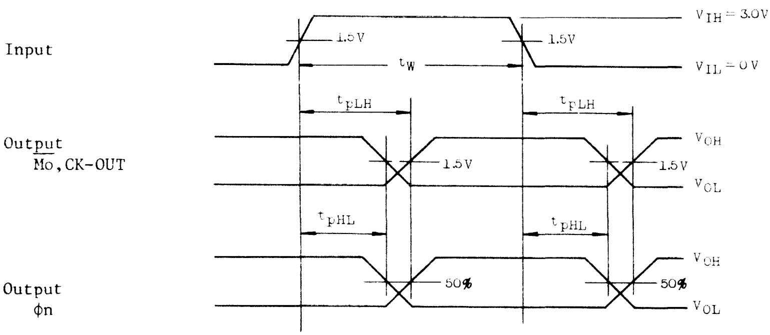
SWITCHING CHARACTERISTICS (Ta=25°C)

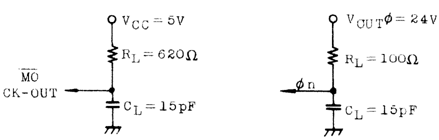
CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Propagation Delay Time, Low-to-High Level	CK-ϕn	t_{pLH}	V_{CC}=5.0V		2.0		μS
	CK–CK-OUT		R_L–CK-OUT, $\overline{Mo}$=620Ω		1.0		
	CK-$\overline{Mo}$		R_L-ϕ_1∿ϕ_4=100Ω		2.8		
	E-ϕn		C_L-All Outputs=15pF		1.0		
	$\overline{R}$-ϕn		$V_{OUT\phi}$=24V		2.0		

TD62803P

SWITCHING CHARACTERISTICS (Ta=25°C)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Propagation Delay Time High-to-Low Level	CK-ϕn	t_{pHL}	V_{CC}=5.0V		1.4		μS
	CK-CK-OUT		R_L-CK-OUT, $\overline{Mo}$=620Ω		0.7		
	CK-$\overline{Mo}$		R_L-ϕ_1∼ϕ_4=100Ω		2.1		
	E-ϕn		C_L-All Outputs = 15pF		1.2		
	$\overline{R}$-ϕn		$V_{OUT}\phi$=24V		1.0		
	$\overline{R}$-$\overline{Mo}$				2.0		
Maximum Clock Frequency		f_{max}			250		kHz
Set Up Time CK, CW/CCW		t_{set-up}			0.1		μS
Hold Time CK, CW/CCW		t_{hold}			0.1		
Minimum Clock Pulse Width		$t_{w(CK)}$			1.0		
Minimum Reset Pulse Width		$t_{w(\overline{R})}$			1.0		





LOAD CIRCUIT

TD62803P

PIN NAMES AND FUNCTIONS

PIN NO.	SYMBOL	NAME	FUNCTION	
1	CW/CCW	Clock Wise/Counter Clock Wise	Direction Control Input	Function Table A
2	EA	Excitation A	Phase Excitation Mode Input	Function Table B
3	EB	Excitation B		
4	3/4	3 Phases/4 Phases	Phase Control Input	
5	$\overline{Mo}$	Monitor Out	Initial Status Output $\overline{Mo}$="L" at Initial State	
6	ϕ_1	ϕ_1 Out	ϕ_1 Output	
7	ϕ_2	ϕ_2 Out	ϕ_2 Output	
8	GND	GND	GND	
9	ϕ_3	ϕ_3 Out	ϕ_3 Output	
10	ϕ_4	ϕ_4 Out	ϕ_4 Output	
11	E	Output Enable	Outputs are Enable at E="H"	
12	CK-OUT	Clock-Out	Clock Output	
13	CK1	Clock In-1	Clock Input 1	Function Table A
14	CK2	Clock In-2	Clock Input 2	
15	$\overline{R}$	Reset	Reset Input	
16	V_{CC}	V_{CC}	V_{CC}	

FUNCTION TABLE A

CK1	CK2	CW/CCW	FUNCTION
↑	H	L	CW
⎍	L	L	Inhibit
H	↑	L	CCW
L	⎍	L	Inhibit
↑	H	H	CCW
⎍	L	H	Inhibit
H	↑	H	CW
L	⎍	H	Inhibit

FUNCTION TABLE B

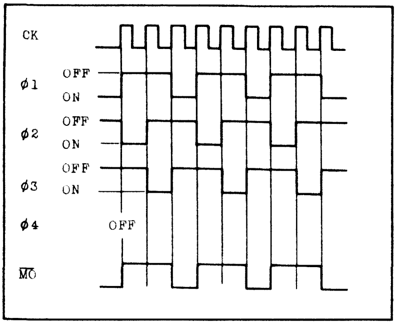
EA	EB	3/4	FUNCTION	
L	L	L	4 Phases	1 Phase Excitation
H	L	L		2 Phase Excitation
L	H	L		1-2 Phase Excitation
H	H	L	Test Mode	$\phi_1 \sim \phi_4$ ON
L	L	H	3 Phases	1 Phase Excitation
H	L	H		2 Phase Excitation
L	H	H		1-2 Phase Excitation
H	H	H	Test Mode	$\phi_1 \sim \phi_4$ ON

NOTE) Conversion of Phase Excitation Mode must be made after the Reset Mode is established.

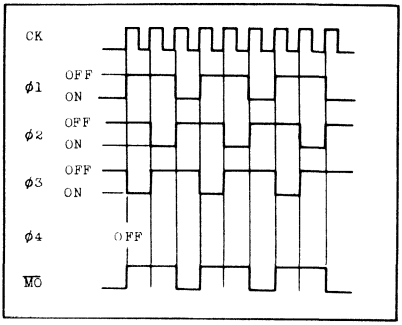
TD62803P

3 PHASES METHOD

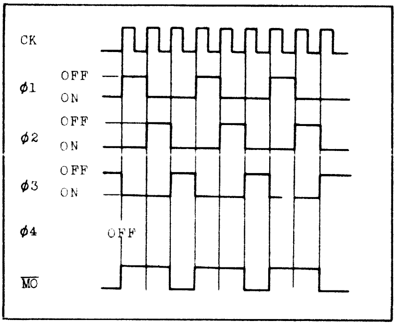
1 PHASE EXCITATION CW



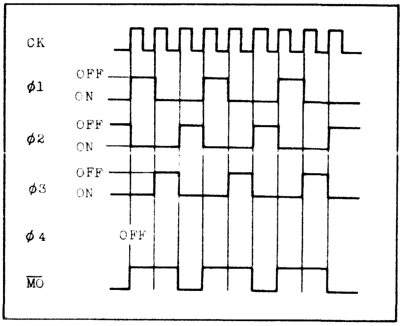
1 PHASE EXCITATION CCW



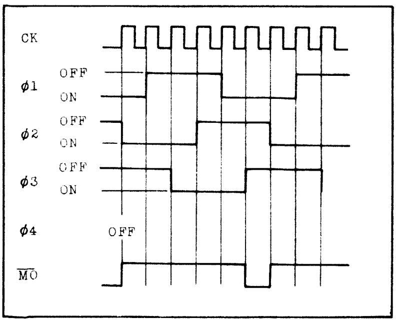
2 PHASE EXCITATION CW



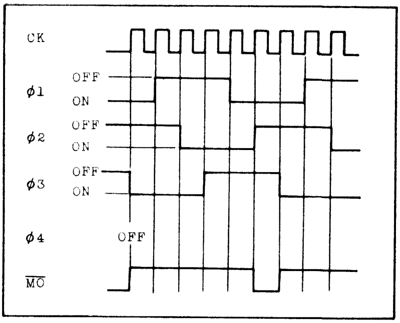
2 PHASE EXCITATION CCW



1-2 PHASE EXCITATION CW



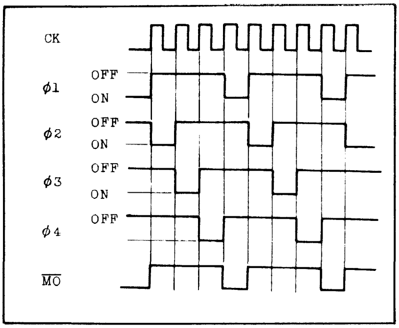
1-2 PHASE EXCITATION CCW



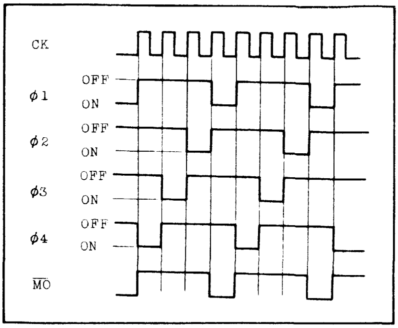
TD62803P

4 PHASES METHOD

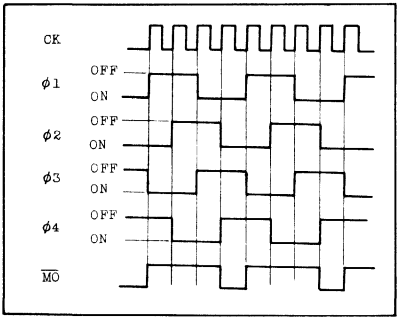
1 PHASE EXCITATION CW



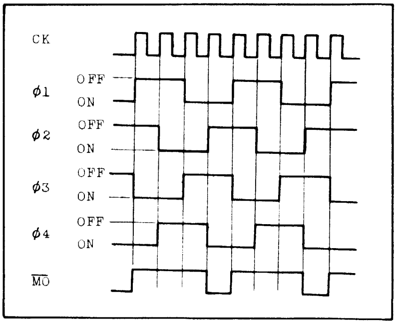
1 PHASE EXCITATION CCW



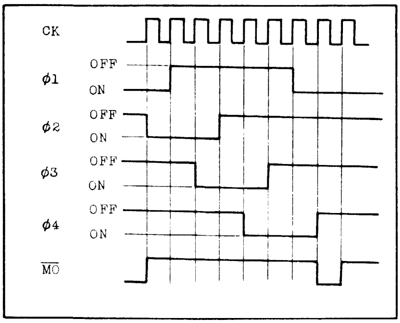
2 PHASE EXCITATION CW



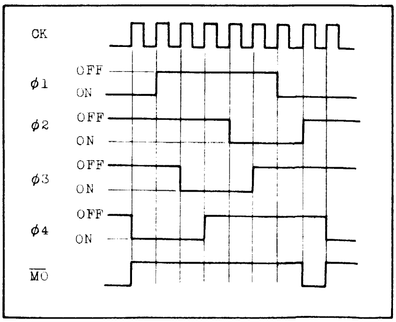
2 PHASE EXCITATION CCW



1-2 PHASE EXCITATION CW



1-2 PHASE EXCITATION CCW



APPLICATIONS INFORMATION

APPLICATIONS INFORMATION

1. TD62001AP Series (TD62001AP, TD62002AP, TD62003AP, TD62004AP)
   TD62081AP Series (TD62081AP, TD62082AP, TD62083AP, TD62084AP)

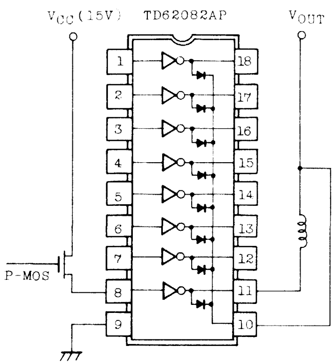
   The TD62001AP/TD62081AP series are the most standard high-voltage, high-current darlington arrays; the TD62001AP series are comprised of seven NPN darlington pairs and the TD62081AP series are comprised of eight NPN darlington pairs. Since all units feature integral clamp diodes, these series are suitable for driving such peripheral components as hammers (printers), relays, solenoids. Needless to say, these series can be used for such non-inductive loads as LED, etc. In this case, clamp diodes can be used for LAMP TEST function because they are not necessary for the circuit configuration.
   The TD62001AP/TD62081AP series contain input current limiting elements and allow operation directly with various types of standard digital IC family (TTL, C-MOS, P-MOS, etc.); and it is possible to select optimum IC according to use.

(1) Recommended Condition

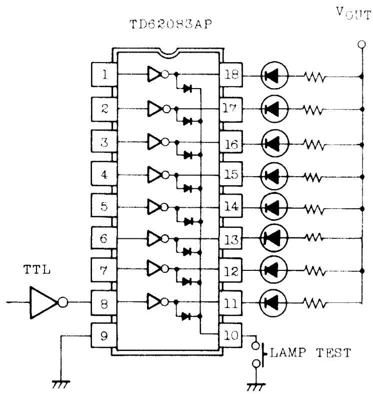
TYPE		INPUT RESISTOR	DESIGNATION
7 CIRCUITS	8 CIRCUITS		
TD62001AP	TD62081AP	No (External)	General Purpose
TD62002AP	TD62082AP	10.5kΩ + 7V Zener Diode	14 ~ 25V P-MOS
TD62003AP	TD62083AP	2.7kΩ	TTL, 5V C-MOS
TD62004AP	TD62084AP	10.5kΩ	6 ~ 15V P-MOS, C-MOS

(2) Typical Application

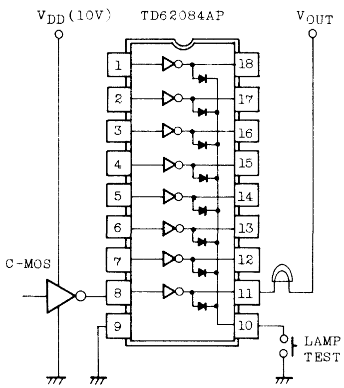
RELAY/SOLENOID/PRINTER DRIVE



LED DRIVE



LAMP DIRVE



Note : When use for LAMP DRIVE, it is necessary to take care of inrush current.
Refer to the following precaution.

(3) Precaution in Application

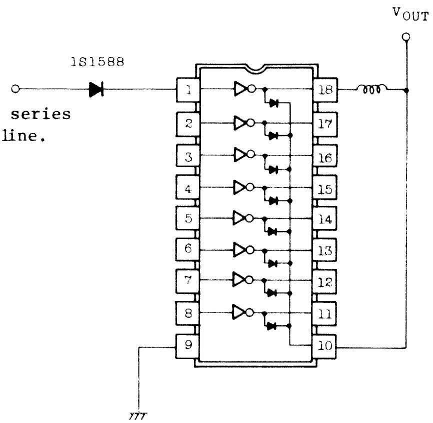
3-1) Precaution for Negative Input Voltage

Most of the transistor array/interface driver family has input parasitic diodes which are produced inevitably from the structure of IC, as discribed in section " Chip Structure and Parasitic Elements".

Therefore, if any negative voltage is applied to the input terminal, forward current flows out through the parasitic diode and function error as well as deterioration of devices can be caused.
In order to protect from negative voltage, discrete diodes should be mounted externally.

Example

Mout a diode in series with the input line.



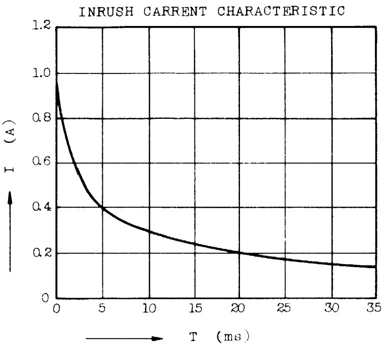
Further, the type numbers which have these diodes internally are the TD62006P, TD62007P, TD62306P and TD62307P.

3-2) Precaution for Inrush Current

When driving lamp loads, it is necessary to take care of inrush current. That is, operating lamp loads requires inrush current as large as approximately 10 times of steady-state when the load is switched ON. Therefore, when a peak value of this inrush current is above the maximum limit of output current, it is necessary to protect the driver.

For example, the characteristic of inrush current is shown on the right side.

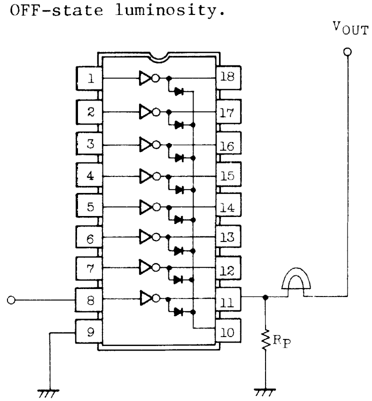
The steady-state current of this lamp is 100mA, but inrush current is approximately 1.0A.



In order to protect the driver it is a general method to insert a resistor for reducing inrush current, and there are following two methode.

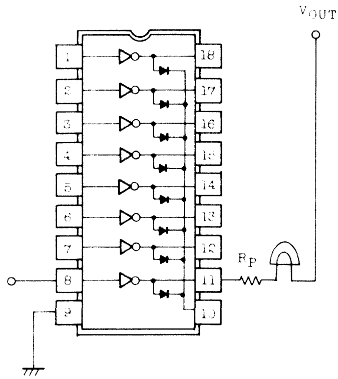
The first method is to reduce inrush current by applying heat current (dark current) which scarecely affects OFF-state luminosity.
In this case, however, power loss in a circuit may become a problem as constant heat current flows.
That is, it may not be possible for some types of lamp to reduce less than 50% of inrush current, unless 20 ~ 30% of steady-state current does not flow.

The second method is to reduce inrush current by inserting a resistor in series with a lamp.



Rp : Inrush current reducing resistor

In this case, if resistance of Rp (an inrush current reducing resistor) is higher than ON resistance of the lamp, luminosity of the lamp decreases; and it is therfor necessary to limit Rp to about several 10% of ON resistance of the lamp.



Rp : Inrush current reducing resistor

3-3) Precaution for Low Avilable Driver Current

In the case of 5V N-ch CPU, for example, TTL fan-out one is normally guranteed for the output characteristics and therefore, source current is specified at only - 200~-400μA while sink current is specified at 1.6mA.

For example, drive from CPU which has following electrical characteristics is considered here.

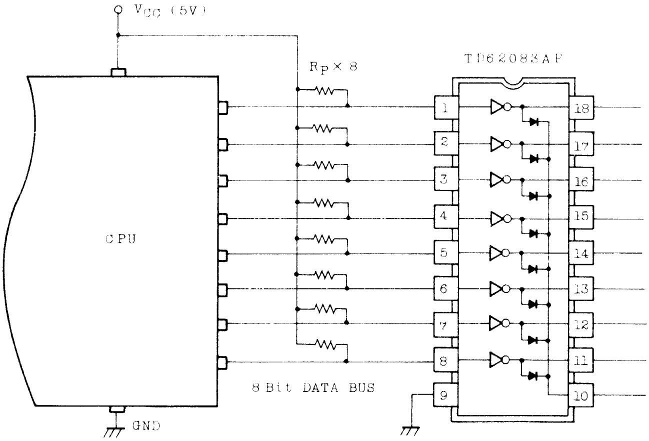
Example

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
"H" Level Output Voltage	V_{OH}	V_{CC}=4.5V, I_{OH}=-400μA	2.4	-	-	V
"L" Level Output Voltage	V_{OL}	I_{OL}=1.8mA	-	-	0.4	V

Since this case is the drive from a standard supply of 5V, use of the TD62083AP (or the TD62003AP) can be considered from "Recommended Condition" but according to the characteristics of I_{IN}-V_{IN}, approximately 0.7mA is at least required for $I_{IN(ON)}$ when V_{IN}=2.4V.

Therefore, under the worst case condition I_{OUT}=350mA can not be guranteed when CPU is directly connected to the driver, and in order to soluve this problem pull-up resistors should be mounted externally as shown in the following figure.



A value of this Rp is

$$\frac{V_{CC\ max}-V_{OL}}{I_{OL}} < R_P < \frac{V_{CC\ min}-V_{IN}}{I_{IN}-|I_{OH}|}$$

$$\frac{(5.5-0.4)V}{1.8mA} < R_P < \frac{(4.5-2.4)V}{(700-400)\mu A}$$

$$2.8k\Omega < R_P < 7k\Omega$$

Therefore, it is generally recommended to use a Rp of 3k ~6kΩ.

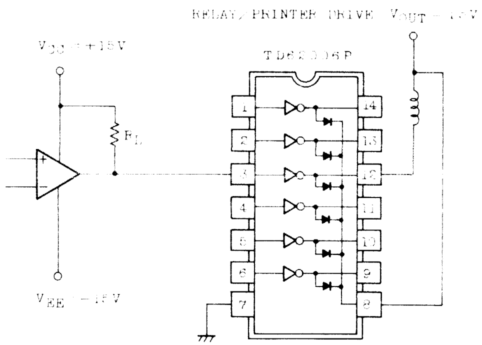
2. TD62006P Series (TD62006P, TD62007P)

The TD62006P is comprised of six NPN darlington pairs and the TD62007P is comprised of seven NPN darlington pairs.
Both darlington transistors are in the same design and electrical characteristics, and only difference between them is the number of circuits (=pacakge).

The recommended operating conditions are output sustaining voltage at 20V and output current at 120mA; and with internal clamp diodes, the TD62006P series are just suitable for driving such inductive loads as small printers, relays, etc.

Futher, this series are also suitable for interfaces between minus and plus dual supply voltage system to plus single supply voltage system because all unit feature internal negative voltage input protective diodes (withstand 35V)

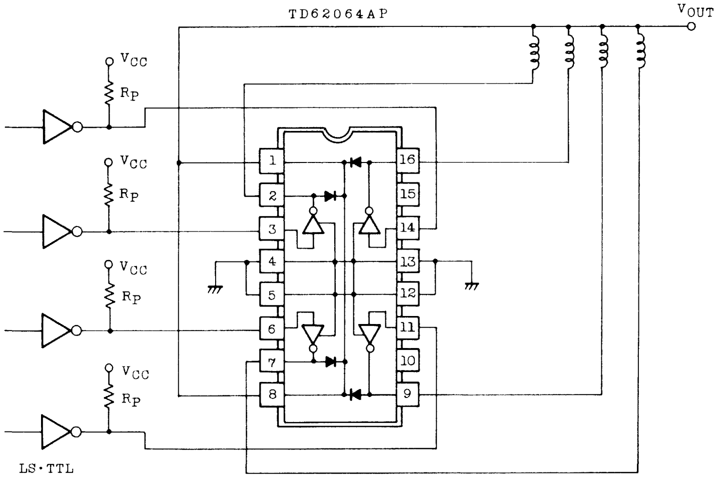
Typical Application



3. TD62064AP Series (TD62064AP, TD62074AP)

The TD62064AP is comprised of four NPN darlington pairs. Since all unit feature integral clamp diodes, the TD62064AP is suitable for driving such inductive loads as hammers (printers), relays, solenoids, and etc.

Typical Application : RELAY DRIVE



In the same caluculating method as in the TD62083AP, the value of this Rp is

$$\frac{V_{CC}\ max - V_{OL}}{I_{OL}} < R_P < \frac{V_{CC}\ min - V_{IN}}{I_{IN} - I_{OH}}$$

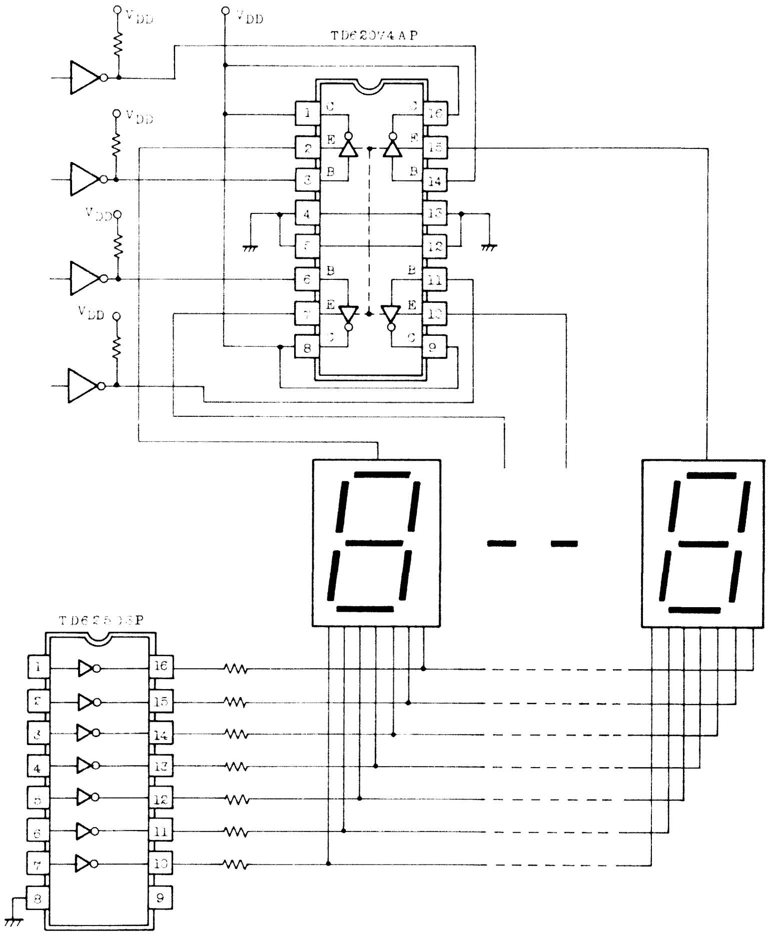
$$\frac{(5.5-0.4)V}{8mA} < R_P < \frac{(4.5-2.4)V}{(2-0.4)mA}$$

$$638\Omega < R_P < 1312\Omega$$

Therefore, it is generally recommended to use a Rp of 1kΩ.

The TD62074 AP is comprised of four NPN darlington pairs. Since all units feature separated each other, it is posible to use this device as a source current driver.

Typical Application : ANODE COMMON LED DRIVE



4. TD62101P Series (TD62101P, TD62103P, TD62104P, TD62105P)

The TD62101P series are comprised of seven NPN darlington pairs and low cost varsion of the TD62001AP series.
Differences between the two series are that the TD62101P series have no internal clamp diode and output sustaining voltage is lower, that is guranteed at 25V.

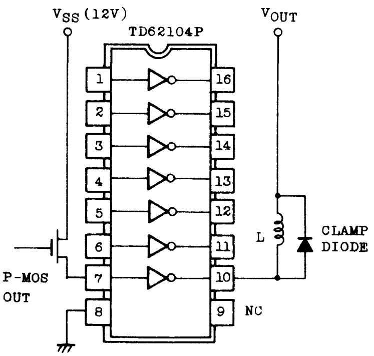
Like TD62001AP series, this series also contain input current limiting elements and allow operation directly with various types of standard digital IC family (TTL, C-MOS, P-MOS, etc.); and it is possible to select optimum IC according to use.

(1) Recommended Condition

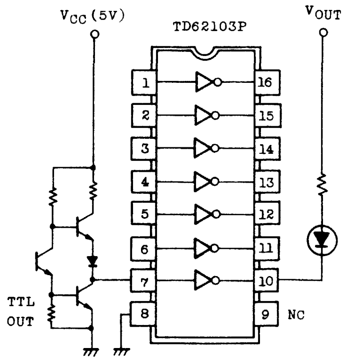
TYPE	INPUT RESISTOR	DESIGNATION
TD62101P	No (External)	General Purpose
TD62103P	2.7kΩ	TTL, 5V C-MOS
TD62104P	10.5kΩ	6 ~ 15V P-MOS, C-MOS
TD62105P	20kΩ	12 ~ 25V P-MOS, C-MOS

(2) Typical Application

RELAY/SOLENOID/PRINTER DRIVE

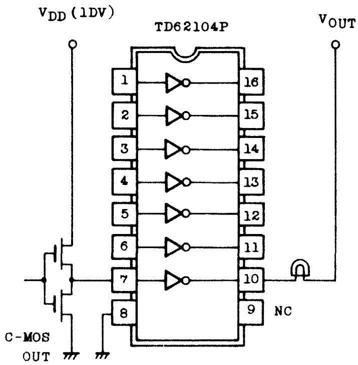


LED DRIVE



Note : In the case of inductive loads, external clamp diode should be connected across the load.

LAMP DRIVE



When used as a lamp drive, it is necessary to take care of inrush current.

(3) Precaution in Application

Refer to the " Precaution in Application" of the TD62001AP series.

5. TD62301P Sèries (TD62301P, TD62302P, TD62306P, TD62307P)

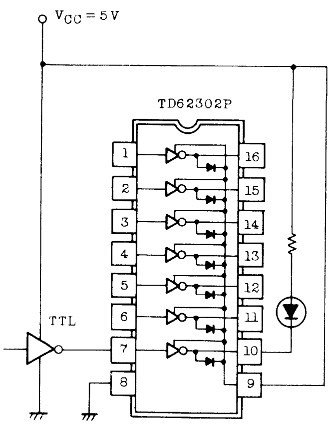
The TD62301P series are NPN low output saturation voltage type transistor arrays. Sine all units feature integral clamp diodes, this series are best suitable for driving such inductive loads as small printers, relays, etc. as well as LEDs and lamps.

(1) Recommended Conditions

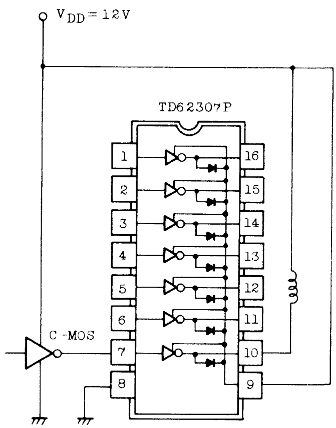
TYPE	INPUT RESISTOR	DESIGNATION
TD62301P	R_{IN}=2kΩ (R_{BE}=20kΩ)	TTL, 3 ~ 6 V C-MOS
TD62302P	R_{IN}=8.4kΩ (R_{BE}=15kΩ)	
TD62306P TD62307P	R_{IN}=20kΩ & Negative voltage protective diode	TTL, 5 ~ 18V C-MOS
It is not recommended to drive the TD62301P and TD62302P by 6 ~ 15V C-MOS circuit from the view point of power dissipation.		

(2) Typical Application

LED DRIVE



RELAY DRIVE

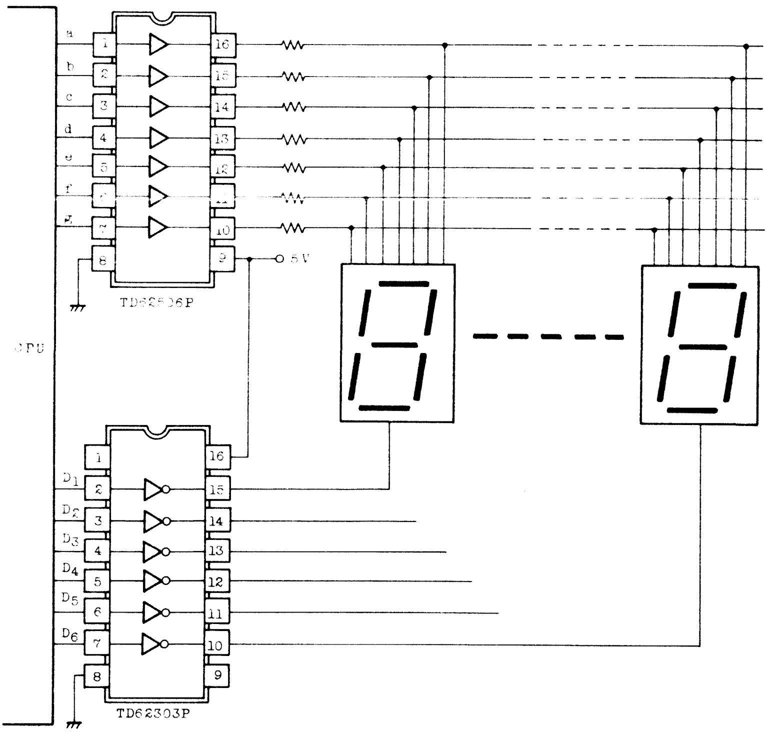


6. TD62303P

The TD62303P is comprised of six NPN low saturation drivers.
This device is specifically designed for multiplexed digit driving of six digits common cathode LED display.
The input can be directly connected with 5V C-MOS and TTL.

The TD62303P also can be used as an interface for a general purpose logic system. In this case, however, for thermal condition it is recommended to limit simultaneous ON to one circuit.

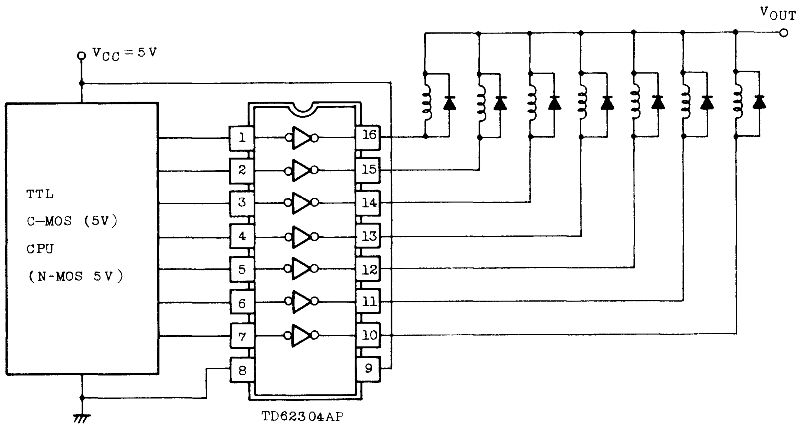
Typical Application : DYNAMIC LED (CATHODE COMMON) DRIVE



7. TD62304AP Series (TD62304AP, TD62305AP, TD62308AP)

The TD62304AP series are non-inverting transistor arrays, which are comprised of seven or four NPN darlington output stages and PNP input stages. These devices are low level input active drivers and are suitable for operation with TTL, 5V C-MOS and CPU which have sink current output.

Typical Application : PRINTER DRIVE

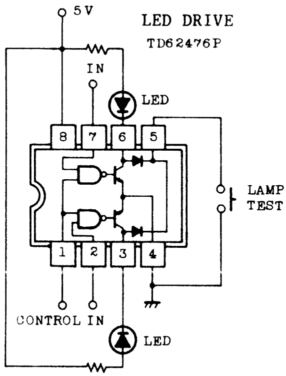


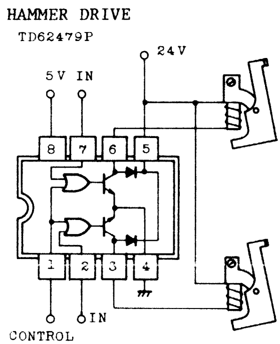
In the case of inductive loads, external clamp diode should be connected across the load.

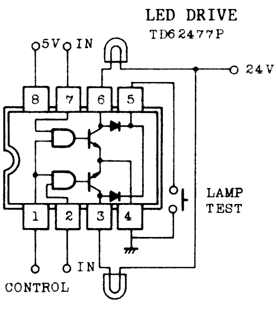
8. TD62476P Series (TD62476P, TD62477P, TD62478P, TD62479P)

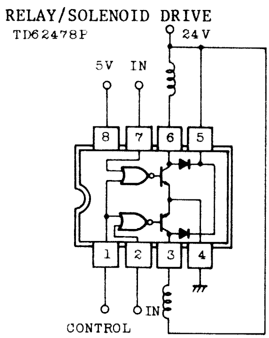
The TD62476P series are dual peripheral drivers consisting of TTL compatible 2 input basic gates (NAND, AND, NOR and OR) and output transistors. Since all units feature integral clamp diodes, this series are suitable for driving such inductive loads as hammers (Printers), relays, solenoide. Obcause they also can be used to drive non-inductive loads such as LED, etc.

(1) Typical Application









(2) Precaution in Application

Refer to "Precaution in Application" of the TD62001AP series.

9. TD62501P Series (TD62501P, TD62502P, TD62503P, TD62504P, TD62505P, TD62506P. TD62507P)

TD62551S Series (TD62551S, TD62553S, TD62554S, TD62555S)

The TD62501P/TD62551S series are comprised of seven or five or four NPN transistor pairs. These series contain internal current limiting elements and they can directly connected from various types of standard digital IC family (TTL, C-MOC, P-MOS, etc.); so it is possible to select optimum IC according to use.

(1) Recommended Condition

TD62501P Series

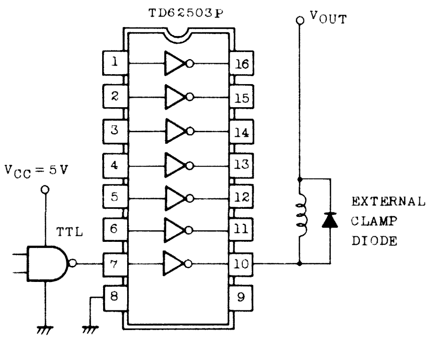
TYPE	No. OF CIRCUITS	COMMON	INPUT RESISTOR	DESIGNATION
TD62501P	7	Emitter	No (External)	General Purpose
TD62505P	7	Collector		
TD62507P	5	Separated		
TD62502P	7	Emitter	10.5kΩ + 7V Z.D.	14 ~ 25V P-MOS
TD62503P	7	Emitter	2.7kΩ	TTL, 5V C-MOS
TD62506P	7	Collector		
TD62504P	7	Emitter	10.5kΩ	6 ~ 15V P-MOS, C-MOS

TD62551S Series

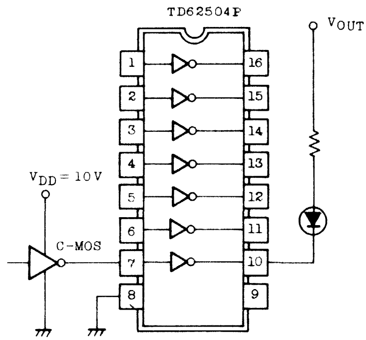
TYPE	No. OF CIRCUITS	COMMON	INPUT RESISTOR	DESIGNATION
TD62551S	4	Emitter	No (external)	General Purpose
TD62553S			2.7kΩ	TTL, 5V C-MOS
TD62554S			10.5kΩ	6 ~ 15V P-MOS, C-MOS
TD62555S			20kΩ	14 ~ 20V P-MOS

(2) Typical Application

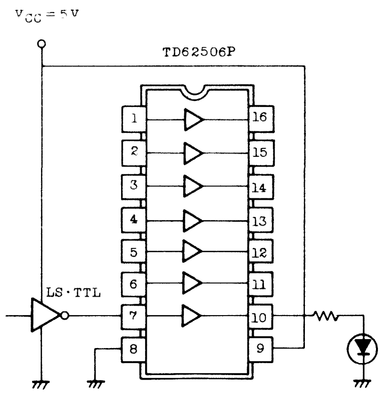
RELAY/SOLENOID/PRINTER DRIVE



LED DRIVE



LED DRIVE



10. TD62703P Series (TD62703P, TD62705P, TD62706P, TD62781AP, TD62782AP)

The TD62703P series are high-voltage, source-current drivers, which are comprised of six or eight circuits.
Since source current is as high as 50mA, this series are best suitable for fluorescent display applications and are also suitable interface between low-level to high-level logic.
Further, the TD62703P series have internal current limiting elements and they can be directly connected to various types of standard digital IC family (TTL, C-MOS, P-MOS, etc.).

(1) Recommended Condition

TYPE	INPUT RESISTOR	V_{CC}	V_{EE}	SUB	DESIGNATION
TD62703P	2.7kΩ	5V		0~ -50V	5V C-MOS
TD62705P	57kΩ	6 ~ 25V	GND	0~ -49V	6 ~ 25V C-MOS, P-MOS
TD62706P	20kΩ	5V	GND	0~ -50V	TTL, 5V C-MOS
TD62781AP	10kΩ (V_{TH}=1.5V)	Each output has internal pull-down resistor			TTL, 5V C-MOS
TD62782AP	10kΩ (V_{TH}=3.5V)				6 ~ 15V C-MOS, P-MOS

Note 1 : The substrate (SUB) should be connected to the most negative voltage.
2 : Use in a range of
$V_{CC}-V_{SUB} \leqq 55V$.....TD62703P, TD62705P, TD62706P
$V_{CC}-GND \leqq 55V$.....TD62781AP, TD62782AP
3 : When the TD62703P is used under the condition of
.V_{CC}=5V, SUB=0 ~ -50V
.TTL or 5V Nch-MOS system
it is necessary to pull-up the inputs in order to keep the V_{IH}
$V_{CC}-1.1V_{BE}=5-0.44=4.56V$

Example : A value of pull-up resistor Rp when the TD62703P is driven by TTL is

$$\frac{V_{CC}-V_{OL}}{I_{OL}} < R_P < \frac{1.1 \times V_{BE(OFF)}}{\text{TTL Lrak}}$$

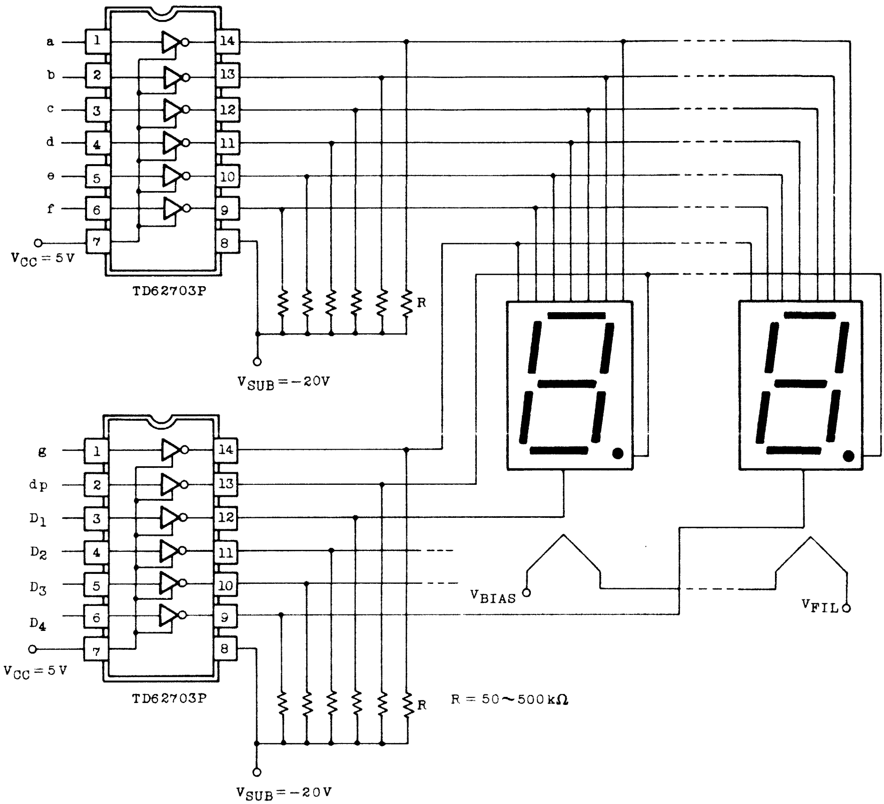
$$\frac{(5-0.4)V}{16mA} < R_P < \frac{1.1 \times 0.4V}{250\mu A}$$

$$288\Omega < R_P < 1760\Omega$$

Therefore, it is generally recommended to use a resistor of 1kΩ.

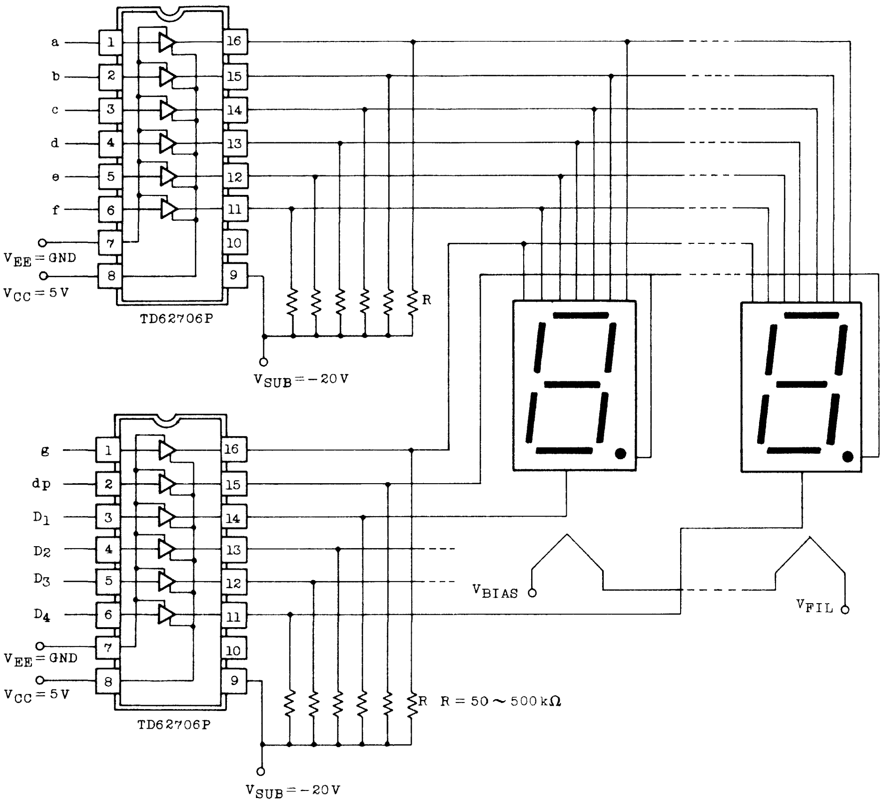
(2) Typical Application

FLUORESCENT DISPLAY APPLICATION I, TD62703P

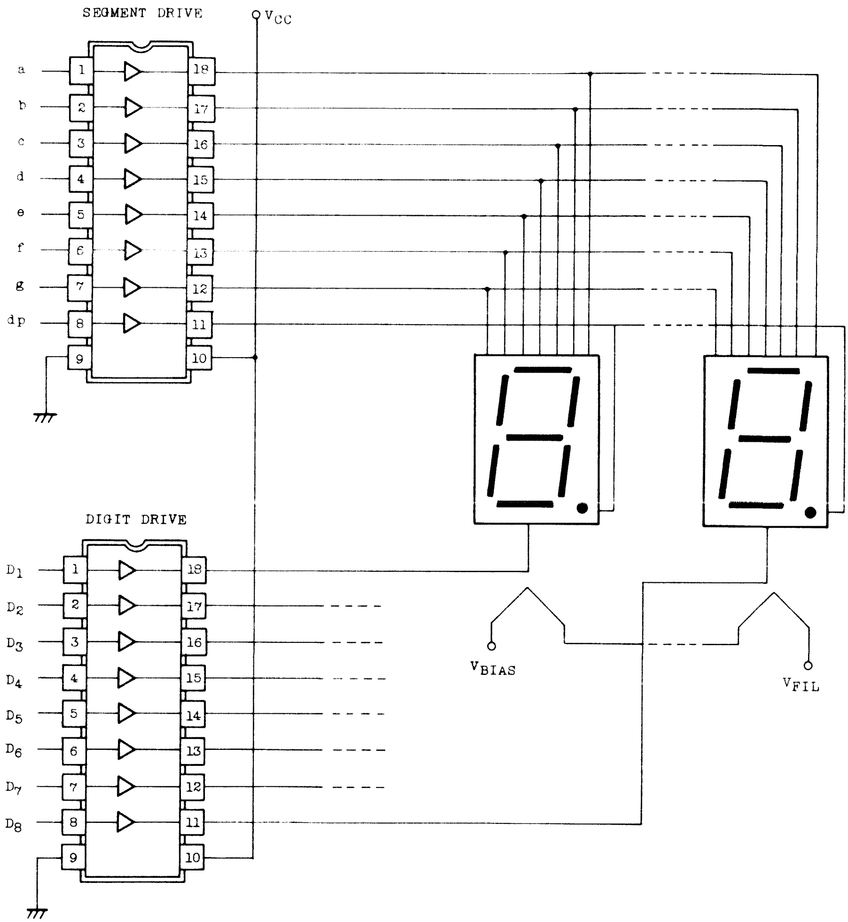


Note : a ~ g, dp, D_1 ~ D_4 inputs are directly driven from 5V C-MOS.

FLUORSCENT DISPLAY APPLICATION II TD62706P



FLUORSCENT DISPLAY APPLICATION Ⅲ   TD62781AP, TD62782AP



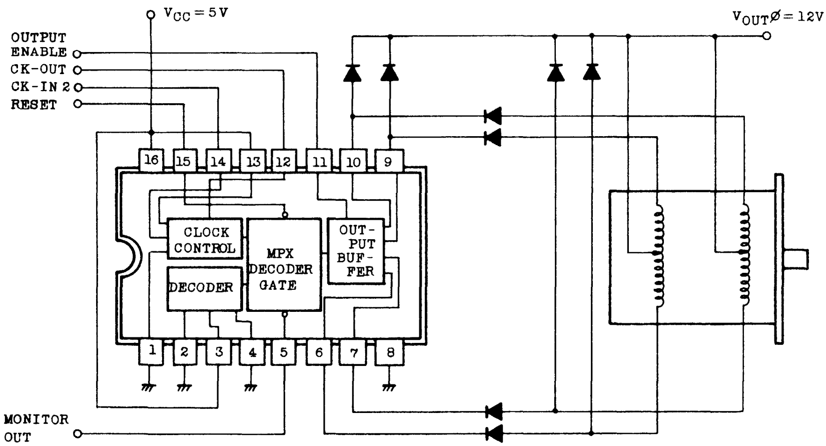
11. TD62803P

The TD62803P is a stepping motor controller/driver IC. This device can be used for both of 3-phase and 4-phase motors and has the CW/CCW (Clock Wise/Counter Clock Wise) rotation and various excitation modes (1, 2, 1-2 phase excitation).

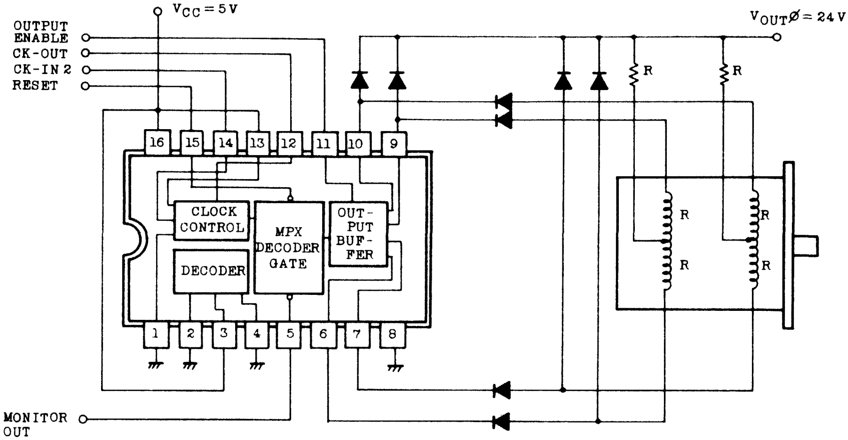
Inputs are all TTL compatible and each phase output has drive capacity of 28V/400mA; therefore, this device is capable of directly driving small-to-medium size stepping motors.

(1) Typical Application

4 PHASE MOTOR, 1-2 PHASE EXCITATION I



4 PHASE MOTOR, 1-2 PHASE EXCITATION II



CROSS REFERENCE

CROSS REFERENCE

TRANSISTOR ARRAY & INTERFACE DRIVER

TOSHIBA	SPRAGUE	TI	MOT	SGS	MITSU-BISHI	SANYO
TD62001AP	ULN2001A	ULN2001A	MC1411P	L201B	M54524P	LB1231
TD62002AP	ULN2002A	ULN2002A	MC1412P	L202B	M54525P	LB1232
TD62003AP	ULN2003A	ULN2003A	MC1413P	L203B	M54523P	LB1233
TD62004AP	ULN2004A	ULN2004A	MC1414P	L204B	M54526P	LB1234
TD62006P					M54527P	LB1274
TD62007P					M54528P	LB1275
TD62064AP	ULN2064B	ULN2064				
TD62074AP	ULN2074B	ULN2074				
TD62081AP	ULN2801A			L601B		
TD62082AP	ULN2802A			L602B		
TD62083AP	ULN2803A			L603B		
TD62084AP	ULN2804A			L604B	M54522P	
TD62101P						
TD62103P						
TD62104P						
TD62105P					M54517P	
TD62107P						
TD62301P					M54537P	LB1261
TD62302P						
TD62303P						
TD62304AP					M54566P	
TD62305AP						
TD62306P					M54533P	LB1269
TD62307P						LB1260
TD62308AP					M54567P	
TD62476P	UDN5711M	SN75476	MC1471P			
TD62477P	UDN5712M	SN75477	MC1472P			
TD62478P	UDN5713M	SN75478	MC1473P			
TD62479P	UDN5714M	SN75479	MC1474P			
TD62501P						LB1211
TD62502P						LB1212
TD62503P						LB1213
TD62504P						LB1214
TD62505P						LB1215
TD62506P						LB1216
TD62507P						LB1217
TD62551S						
TD62553S						
TD62554S						
TD62555S						
TD62601P						
TD62602P						
TD62603P						
TD62604P						
TD62703P	UHP495					
TD62705P	UHP491					
TD62706P						
TD62781AP	UDN6118A					LB1290
TD62782AP	UDN6128A					LB1291
TD62801P						
TD62803P						

Operational Amplifier

Voltage Comparator

Series

ALPHANUMERIC INDEX

Operational Amplifier/Voltage Comparator/Timer

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TA75902P 231

SELECTION GUIDE

FUNCTIONAL INDEX/SELECTION GUIDE

OPERATIONAL AMPLIFIER, VOLTAGE COMPARATOR, TIMER

FUNCTION			DIP	SIP	FLP
OP AMP.	General Purpose	Single	TA7502P		
			TA7504P	TA7504S	
			TA7506P		
		Dual	TA75358P		* TA75358F
			TA75458P	TA75458S	* TA75458F
		Quad	TA75902P		* TA75902F
	Low Drift	Single	* TA75254P		
	Micro Power	Single	* TA7540P		
	Low Noise	Dual	TA75557P	TA75557S	* TA75557F
			TA75558P	TA75558S	* TA75558F
			TA75559P	TA75559S	* TA75559F
COMPARATOR		Single		TA7523S	
				TA7523AS	
		Dual	TA75393P	TA75393S	* TA75393F
			* TA75393AP	* TA75393AS	
		Quad	TA75339P		* TA75339F
			* TA75339AP		
TIMER		Single	TA7555P		* TA7555F

* New Product or Under Development

AP, AS: Hihg Sink Current Type. (60mA)

TECHNICAL DATA SHEET

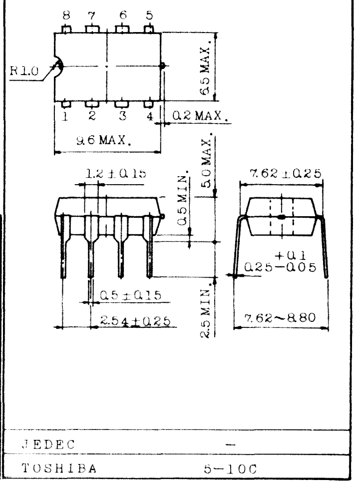
BIPOLAR LINEAR INTEGRATED CIRCUIT
SILICON MONOLITHIC

TA7502P

SINGLE OPERATIONAL AMPLIFIER
OPERATIONAL AMPLIFIER
DC AMPLIFIER

. High Gain
. Low Input Offset Voltage : V_{IO}=0.5mV (Typ.)

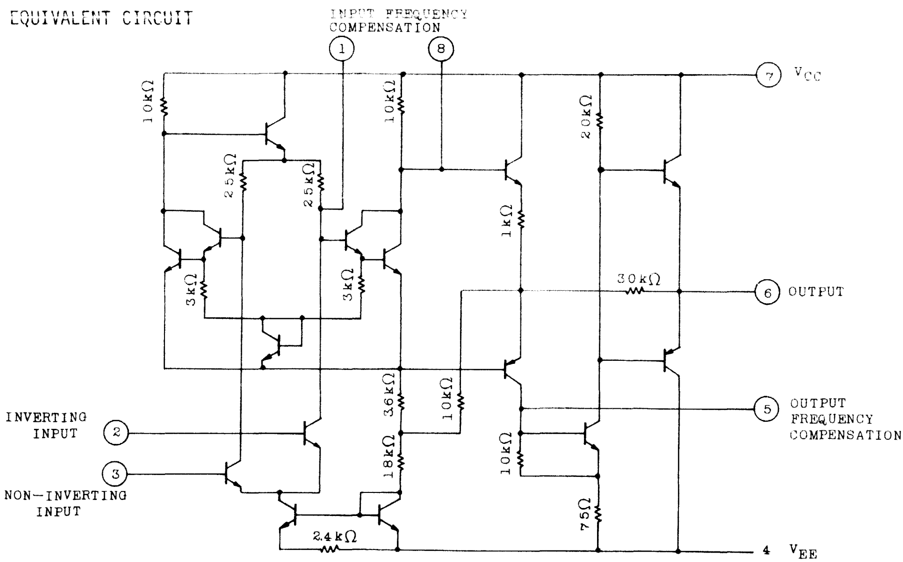
Unit in mm



MAXIMUM RATINGS (Ta=25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}, V_{EE}	±18	V
Power Dissipation	P_D	300	mW
Differential Input Voltage	DV_{IN}	6	V
Input Voltage (V_{CC}, V_{EE}=±15V)	V_{IN}	+10 -15	V
Output Short Circuit Current	I_{OS}	±20	mA
Operating Temperature	Topr	-30 ~ 75	°C
Storage Temperature	Tstg	-55 ~ 125	°C

EQUIVALENT CIRCUIT



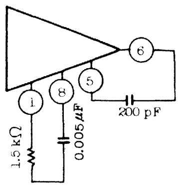
TA7502P

ELECTRICAL CHARACTERISTICS (V_{CC}=15V, V_{EE}=-15V, Ta=25°C)

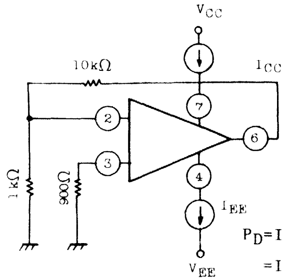
CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	V_{IO}	2	$R_g \leq 10k\Omega$	-	-	5	mV
Input Offset Current	I_{IO}	3	-	-	50	150	nA
Input Bias Current	I_I	3	-	-	200	500	nA
Input Impedance	Z_{IN}	-	f=1kHz	150	380	-	kΩ
Output Impedance	Z_O	-	f=1kHz	-	150	-	Ω
Voltage Gain	G_V	5	$R_L \geq 2k\Omega$, f=1kHz $V_{OUT}=\pm10V$	20	45	-	$\times10^3$
Maximum Output Voltage	V_{OM}	4	$R_L \geq 10k\Omega$	±12	±14	-	V
	V_{OMR}		$R_L \geq 2k\Omega$	±10	±13	-	
Maximum Output Voltage Swing	V_{Op-p}	5	$R_L = 10k\Omega$, f=1kHz	24	28	-	V
Common Mode Input Voltage	CMV_{IN}	6	-	+9 -12	+10 -13	-	V
Common Mode Input Signal Rejection Ratio	CMRR	6	f=1kHz	70	90	-	dB
Supply Voltage Rejection Ratio	SVRR	2	$R_g=10k\Omega$	-	25	100	μV/V
Power Dissipation	P_D	1	-	-	80	150	mW
Input Noise Voltage	e_{np-p}	7	$R_g=10k\Omega$, f=0 ~100Hz	-	-	20	μV
Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	2	$R_g \leq 100\Omega$, Ta=-30~75°C	-	-	20	μV/°C

TA7502P

TEST CIRCUIT



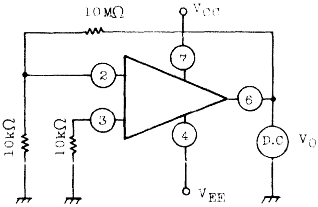
(1) P_D



$P_D = I_{CC}(V_{CC} - V_{EE})$

$= I_{EE}(V_{CC} - V_{EE})$

(2) V_{IO}, SVRR



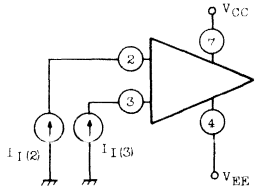
$V_{IO} = V_{OUT}/1000$

$SVRR = (V_{OUT1} - V_{OUT2})/5000$

V_{OUT1}: $V_{CC} = V_{EE} = 17.5V$

V_{OUT2}: $V_{CC} = V_{EE} = 12.5V$

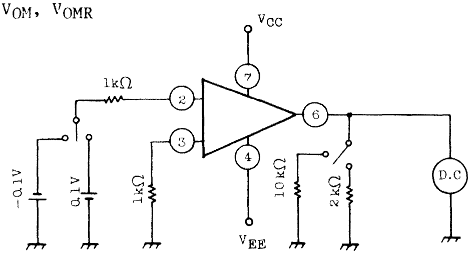
(3) I_I, I_{IO}



$I_I = \frac{I_{I(-)} + I_{I(+)}}{2}$

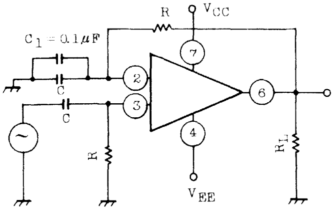
$I_{IO} = |I_{I(-)} - I_{I(+)}|$

(4) V_{OM}, V_{OMR}



TA7502P

(5) G_V, V_{Op-p}



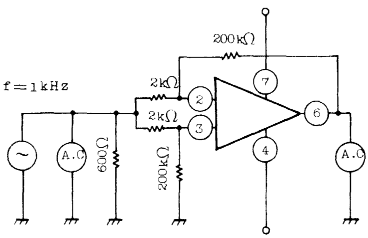
C : DC COUPLE

C_1 : HF BYPASS

$\omega \gg 1/RC$

$G_V = V_{OUT}/V_{IN}$

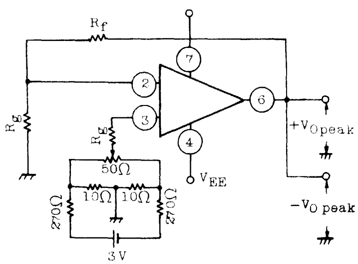
(6) CMRR, CMV_{IN}



$$CMRR = 20\ \ell og\ \frac{70.7}{V_{OUT}}\ (dB)$$

$V_{IN} = 0.707$ (V_{rms})

(7) e_{np-p}



AFTER ADJUSTING BY VR,

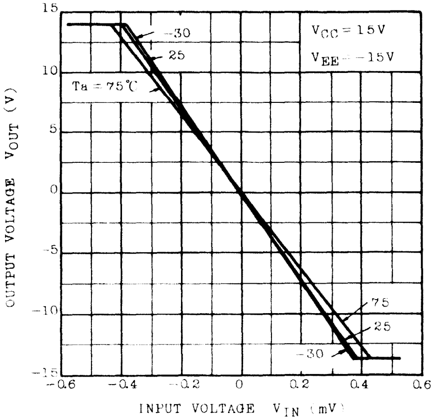
BEING TESTED $+V_{Opeak}$, $-V_{Opeak}$

e_{np-p}

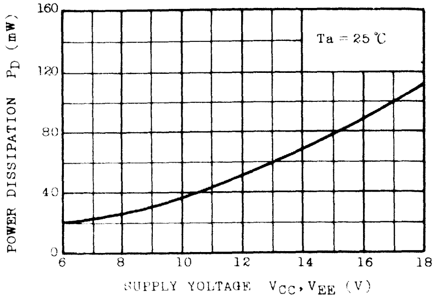
$$= \frac{R_g}{R_f}(|+V_{Opeak}|+|-V_{Opeak}|)$$

TA7502P

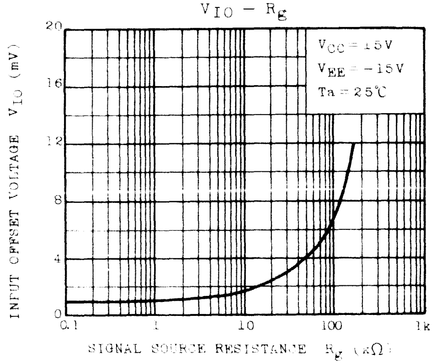
$V_{OUT} - V_{IN}$



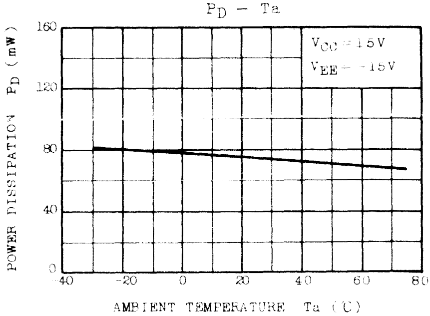
$P_D - V_{CC}, V_{EE}$



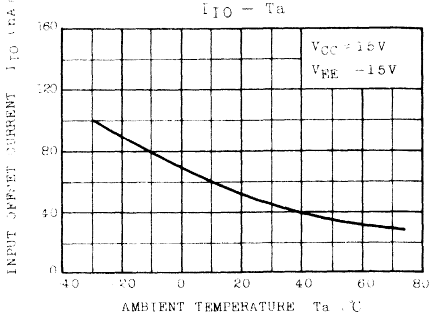
$V_{IO} - R_g$



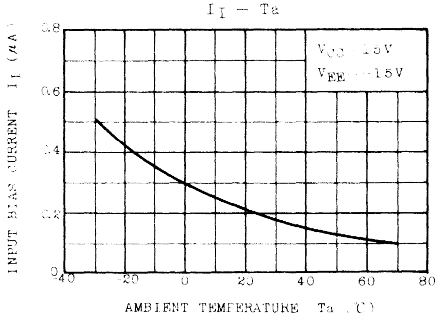
$P_D - Ta$



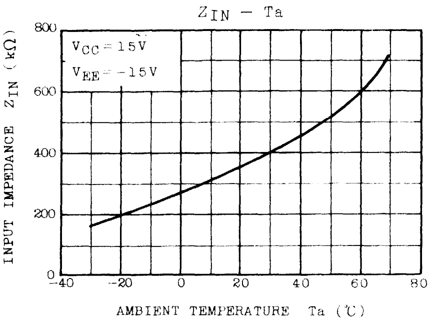
$I_{IO} - Ta$

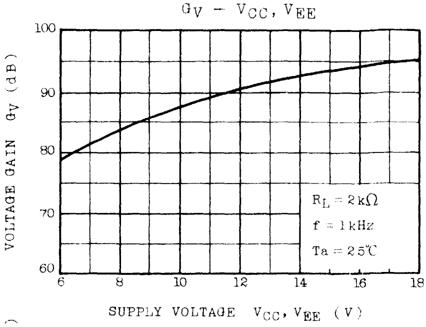


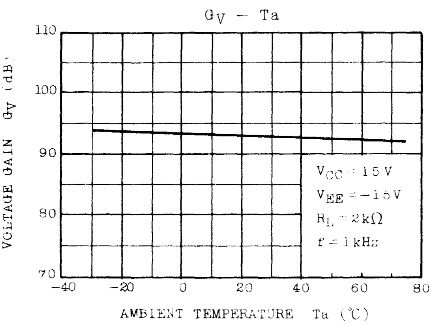
$I_I - Ta$

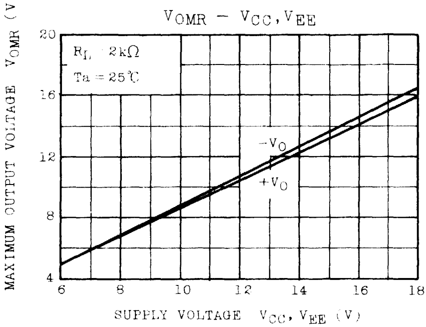


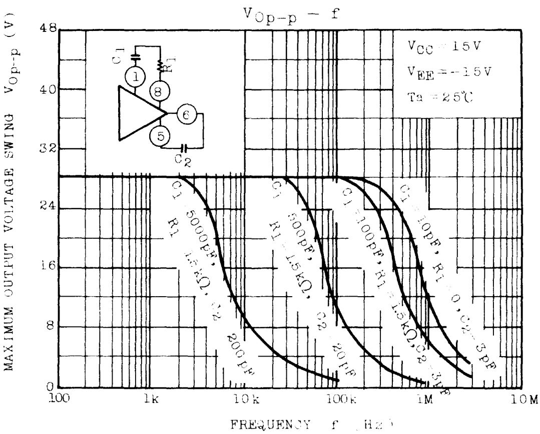
TA7502P

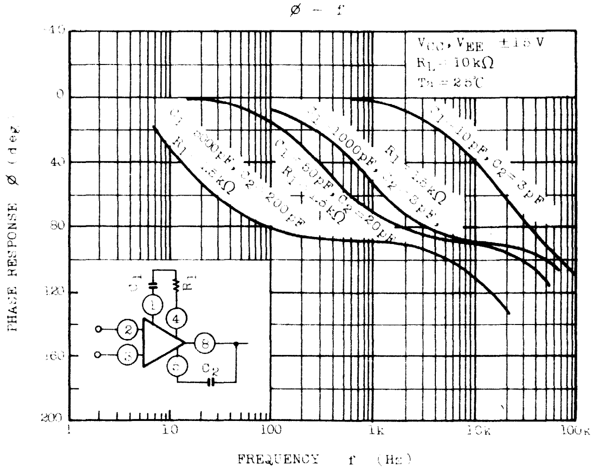

Z_{IN} − Ta
INPUT IMPEDANCE Z_{IN} (kΩ)
AMBIENT TEMPERATURE Ta (℃)
V_{CC} = 15V
V_{EE} = −15V
800
600
400
200
0
−40
−20
0
20
40
60
80

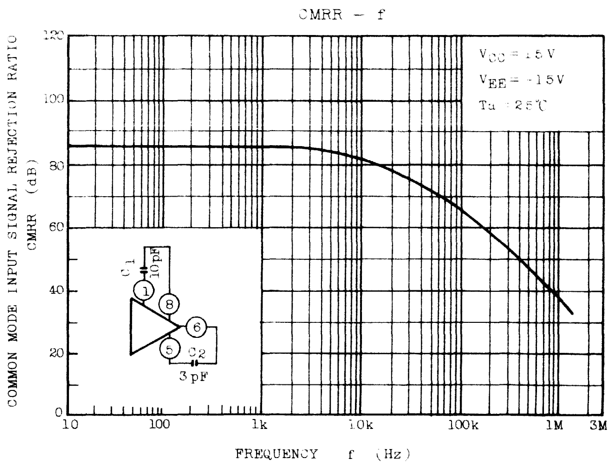

G_V − V_{CC}, V_{EE}
VOLTAGE GAIN G_V (dB)
SUPPLY VOLTAGE V_{CC}, V_{EE} (V)
R_L = 2kΩ
f = 1kHz
Ta = 25℃
100
90
80
70
60
6
8
10
12
14
16
18


G_V − Ta
VOLTAGE GAIN G_V (dB)
AMBIENT TEMPERATURE Ta (℃)
V_{CC} = 15V
V_{EE} = −15V
R_L = 2kΩ
f = 1kHz
110
100
90
80
70
−40
−20
0
20
40
60
80

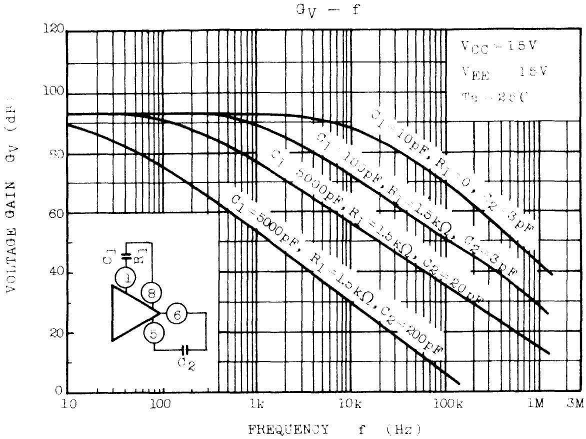

V_{OMR} − V_{CC}, V_{EE}
MAXIMUM OUTPUT VOLTAGE V_{OMR} (V)
SUPPLY VOLTAGE V_{CC}, V_{EE} (V)
R_L = 2kΩ
Ta = 25℃
$-V_O$
$+V_O$
20
16
12
8
4
6
8
10
12
14
16
18

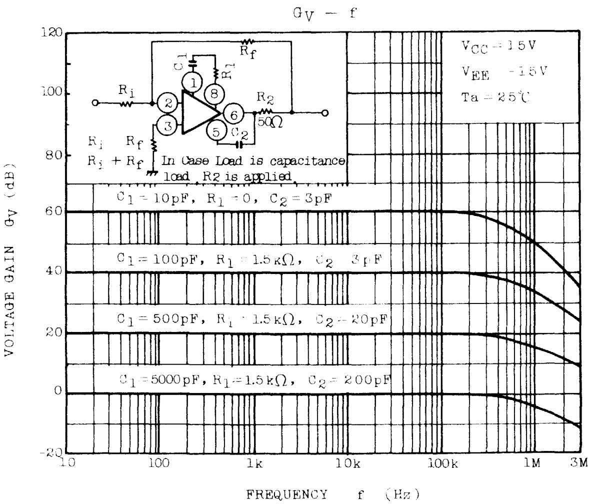

V_{Op-p} − f
MAXIMUM OUTPUT VOLTAGE SWING V_{Op-p} (V)
FREQUENCY f (Hz)
V_{CC} = 15V
V_{EE} = −15V
Ta = 25℃
C_1
R_1
C_2
1
8
6
5
C_1 = 5000pF, R_1 = 1.5kΩ, C_2 = 200pF
C_1 = 500pF, R_1 = 1.5kΩ, C_2 = 20pF
C_1 = 100pF, R_1 = 1.5kΩ, C_2 = 3pF
C_1 = 10pF, R_1 = 0, C_2 = 3pF
48
40
32
24
16
8
0
100
1k
10k
100k
1M
10M


Ø – f
V_{CC}, V_{EE} ±15 V
R_L = 10 kΩ
Ta = 25°C
PHASE RESPONSE Ø (deg)
-40
0
40
80
120
160
200
1
10
100
1k
10k
100k
FREQUENCY f (Hz)
C1 = 30pF, C2 = 3pF
C1 = 1000pF, R1 = 1.5kΩ, C2 = 3pF
C1 = 10pF, C2 = 3pF
C1 = 30pF, R1 = 1.5kΩ, C2 = 20pF
R1 = 1.5kΩ, C2 = 200pF

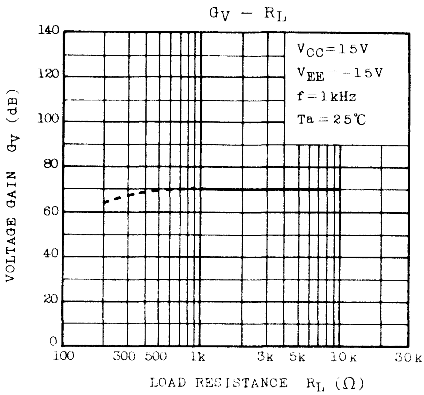

CMRR – f
V_{CC} = 15 V
V_{EE} = -15 V
Ta = 25°C
COMMON MODE INPUT SIGNAL REJECTION RATIO CMRR (dB)
0
20
40
60
80
100
120
10
100
1k
10k
100k
1M
3M
FREQUENCY f (Hz)
C1
10pF
C2
3 pF

TA7502P

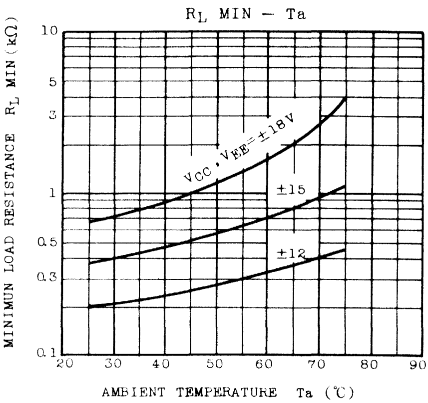

G_V – f
VOLTAGE GAIN G_V (dB)
FREQUENCY f (Hz)
V_{CC} = 15V
V_{EE} = 15V
Ta = 25°C
C_1 = 10pF, R_1 = 0, C_2 = 3pF
C_1 = 100pF, R_1 = 1.5kΩ, C_2 = 3pF
C_1 = 500pF, R_1 = 1.5kΩ, C_2 = 20pF
C_1 = 5000pF, R_1 = 1.5kΩ, C_2 = 200pF
C_1
R_1
C_2
1
8
6
5


G_V – f
VOLTAGE GAIN G_V (dB)
FREQUENCY f (Hz)
V_{CC} = 15V
V_{EE} = -15V
Ta = 25°C
R_i
R_f
R_2
50Ω
C_1
R_1
C_2
$\frac{R_i + R_f}{R_i}$
In Case Load is capacitance load, R2 is applied
C_1 = 10pF, R_1 = 0, C_2 = 3pF
C_1 = 100pF, R_1 = 1.5kΩ, C_2 = 3pF
C_1 = 500pF, R_1 = 1.5kΩ, C_2 = 20pF
C_1 = 5000pF, R_1 = 1.5kΩ, C_2 = 200pF

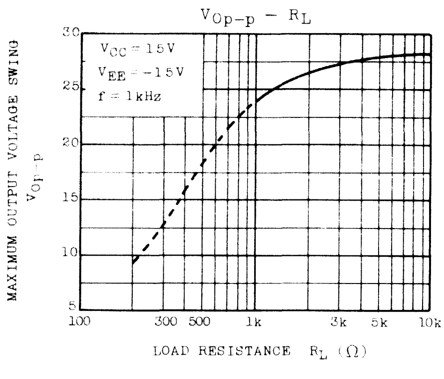
TA7502P



G_V – R_L
V_{CC}=15V
V_{EE}=−15V
f=1kHz
Ta=25℃
VOLTAGE GAIN G_V (dB)
140
120
100
80
60
40
20
0
100
300
500
1k
3k
5k
10k
30k
LOAD RESISTANCE R_L (Ω)



R_L MIN – Ta
MINIMUN LOAD RESISTANCE R_L MIN (kΩ)
V_{CC}, V_{EE}=±18V
±15
±12
10
5
3
1
0.5
0.3
0.1
20
30
40
50
60
70
80
90
AMBIENT TEMPERATURE Ta (℃)



V_{Op-p} – R_L
V_{CC}=15V
V_{EE}=−15V
f=1kHz
MAXIMUM OUTPUT VOLTAGE SWING V_{Op-p}
30
25
20
15
10
5
100
300
500
1k
3k
5k
10k
LOAD RESISTANCE R_L (Ω)

TA7502P

INPUT OFFSET VOLTAGE ADJUSTMENT

The input offset voltage of the TA7502P can easily be nulled,as shown in Fig.1 (a) In this way its stability directly depends on power supply stability. The other power supply V_{BB} should be added, as shown in Fig.1 (b), when power supply of operational amplifier is unregulated.

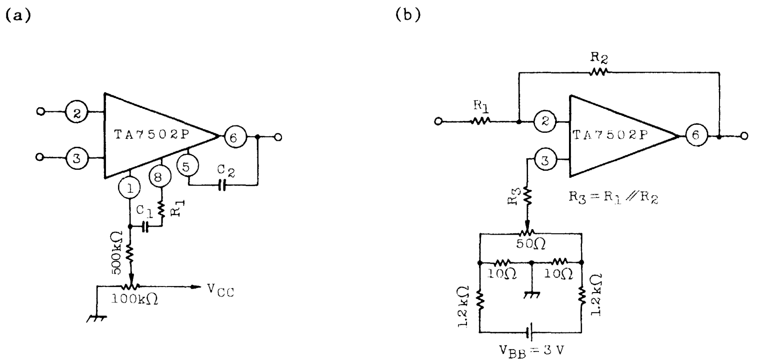


Fig. 1 OFFSET VOLTAGE ADJUSTMENTS

HYSTERESIS PREVENTION

The TA7502P has hysteresis at the positive area in its transfer characteristics. Because when voltage at Term.2 exceeds voltage at Term.1 (about 10V), the transistor in IC chip will be saturated and occur a kind of oscillation phenomenon by becoming positive feedback loop.

It is called "Latch up" and the TA7502P may give rise to abnormal behavior or catastrophic failure under this condition.

To protect against damage from latch up, a diode should be added between Term. 6 and Term. 8, as shown in Fig. 3 (a) and a resistor R should be added in series with feedback loop in Voltage follower application.

TA7502P

The TA7502P has a wide range of common mode input voltage (±9V), and its lineality is guranteed 9 volts in the electrical characteristics. Furthermore, it is possible to improve input voltage ranges by changing power supply voltage, as shown in Table 1.

(a) (b)

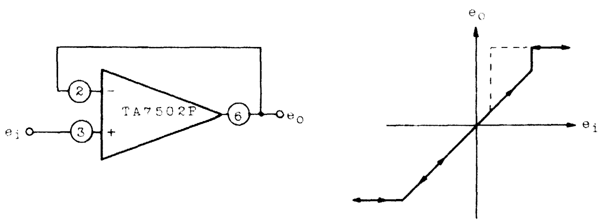
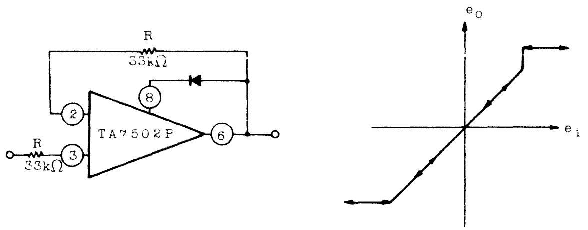


Fig. 2 BASIC VOLTAGE FOLLOWER AND TRANSFER CHARACTERISTIC



(a) VOLTAGE FOLLOWER FREE FROM LATCH UP (b) INPUT/OUTPUT CHARACTERISTICS

V_{CC} (V)	V_{EE} (V)	$CMV_{IN(+)}$ (V)	$CMV_{IN(-)}$ (V)
+5	-25	+1.4	-23.7
+10	-20	+6.0	-18.5
+15	-15	+11.0	-13.7
+20	-10	+15.9	-8.6
+25	-5	+21.1	-3.8

TABLE 1. SUPPLY VOLTAGE-COMMON MODE VOLTAGE

TA7502P

OVERLOAD PROTECTION

Input Protection against differential signal up to the levels of the maximum differential voltage can be provided by the diode clamps of Fig. 4.

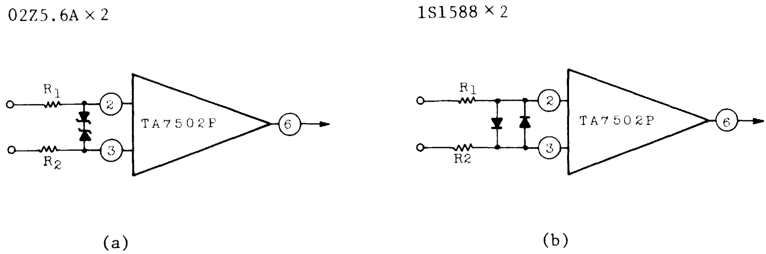


Fig. 4 INPUT PROTECTION AGAINST DIFFERENTIAL INPUT OVERLOAD

OUTPUT SHORT CIRCUIT PROTECTION

The TA7502P endure short circuit current of 80mA maximum for five second at 25°C ambient temperature without degradation. The circuit in Fig. 6 is applied to protect TA7502P from long time short current.

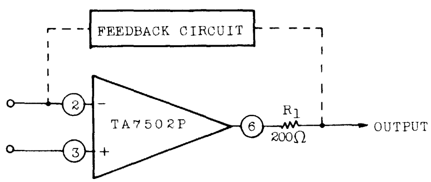


Fig. 5 OUTPUT SHORT CIRCUIT PROTECTION

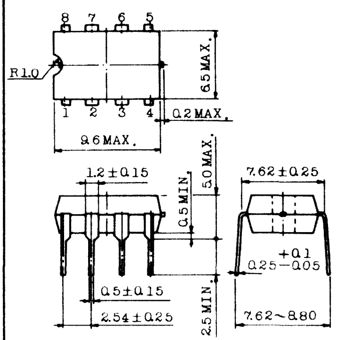
BIPOLAR LINEAR INTEGRATED CIRCUIT
SILICON MONOLITHIC

TA7504P, TA7504S

SINGLE OPERATIONAL AMPLIFIER
OPERATIONAL AMPLIFIER
DC AMPLIFIER

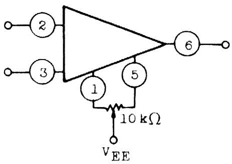
- High Gain : $G_V=1\times10^5$ (Typ.)
- Low Power Dissipation : P_D=50mW (Typ.)
- High Common Mode Input Voltage : $CMV_{IN}=\pm13V$ (Typ.)
- High Differential Input Voltage: DV_{IN}=30 (Typ.)
- Low Input Offset Voltage : V_{IO}=1mV (Typ.)
- No Frequency Compensation
- Absence of Latch-up
- Offset Null Capability
- Short Circuit Protection

Unit in mm

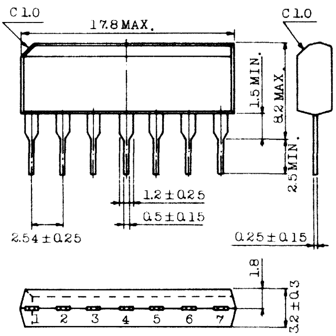


JEDEC	—
TOSHIBA	5−10C

VOLTAGE OFFSET NULL CIRCUIT



Unit in mm



Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 lead.

JEDEC	—
TOSHIBA	5−18A

MAXIMUM RATINGS (Ta=25°C)

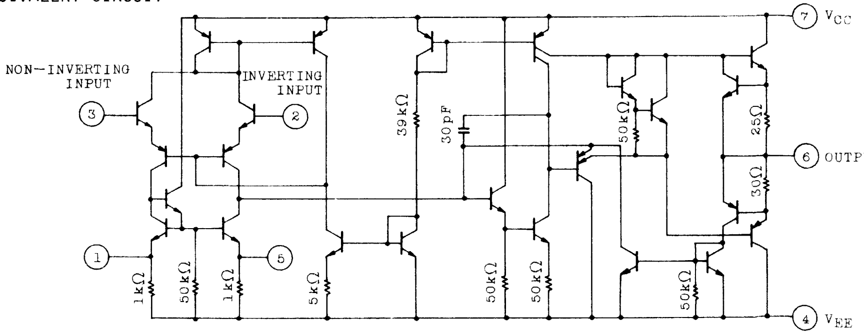
CHARACTERISTIC		SYMBOL	RATING	UNIT
Supply Voltage		V_{CC}, V_{EE}	±18	V
Differential Input Voltage		DV_{IN}	±30	V
Input Voltage		V_{IN}	$V_{CC}\sim V_{EE}$	V
Power Dissipation	TA7504P	P_D	300	mW
	TA7504S		400	
Operating Temperature		T_{opr}	-30 ~75	°C
Storage Temperature		T_{stg}	-55 ~125	°C

TA7504P, TA7504S

ELECTRICAL CHARACTERISTICS (V_{CC}=15V, V_{EE}=-15V, Ta=25°C)

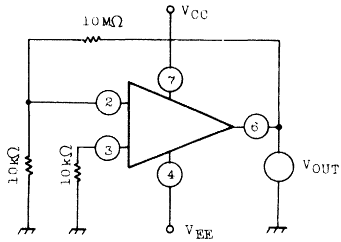
CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	V_{IO}	1	$R_g \leqq 10k\Omega$	-	1	5	mV
Input Offset Current	I_{IO}	2	-	-	30	200	nA
Input Bias Current	I_I	2	-	-	200	500	nA
Common Mode Input Voltage	CMV_{IN}	3	-	±12	±13	-	V
Maximum Output Voltage	V_{OM}	4	$R_L \geqq 10k\Omega$	±12	±14	-	V
	V_{OMR}		$R_L \geqq 2k\Omega$	±10	±13	-	
Maximum Output Voltage Swing	V_{Op-p}	5	R_L=10kΩ, f=1kHz	24	28	-	V
Output Short Circuit Current	I_{OS}	4	-	-	±20	-	mA
Input Impedance	Z_{IN}	-	f=1kHz	0.3	1	-	MΩ
Output Impedance	Z_{OUT}	-	f=1kHz	-	60	-	Ω
Voltage Gain	G_V	-	R_L=2kΩ, V_{OUT}=±10V f=10kHz	20	100	-	$\times 10^3$
Common Mode Input Signal Rejection Ratio	CMRR	3	CMV_{IN}=±10V, f=100Hz	70	90	-	dB
Supply Voltage Rejection Ratio	SVRR	1	$R_g \leqq 10k\Omega$	-	30	150	μV/V
Power Dissipation	P_D	6	-	-	50	85	mW
Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	1	$R_g \leqq 10k\Omega$, Ta=-30 ~ 75°C	-	5	50	μV/°C
Slew Rate	SR	7	R_L=2kΩ	-	0.5	-	V/μs
Rise Time	t_r	8	C_L=100pF, R_L=2kΩ	-	0.3	-	μs
Over Short	e_{over}			-	5	-	%
Input Noise Voltage	e_{np-p}	9	R_g=10kΩ, f=0 ~100Hz	-	6	-	μV

EQUIVALENT CIRCUIT



TEST CIRCUIT

(1) V_{IO}, $\Delta V_{IO}/\Delta T$, SVRR



$V_{IO}=V_{OUT}/1000$

$$SVRR = \frac{V_{OUT}-V_{OUT2}}{1000 \times 5}$$

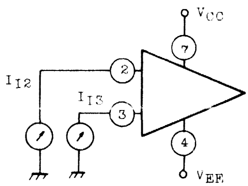
V_{OUT1} ; (V_{CC}, $-V_{EE}$ = 17.5(V)

V_{OUT2} ; (V_{CC}, $-V_{EE}$ = 12.5(V)

$\Delta V_{IO}/\Delta T = |V_{IO}(25^{\circ}C)-V_{IO}(-30^{\circ}C)|/55$

$\Delta V_{IO}/\Delta T = |V_{IO}(25^{\circ}C)-V_{IO}(75^{\circ}C)|/50$

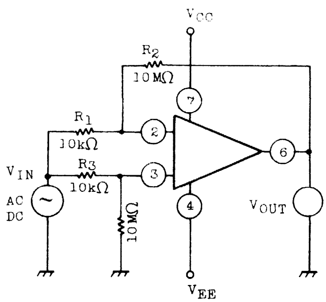
(2) I_I, I_{IO}



$I_{IO}=|I_{I2}-I_{I3}|$

$$I_I = \frac{I_{I2}+I_{I3}}{2}$$

(3) CMV_{IN}, CMRR



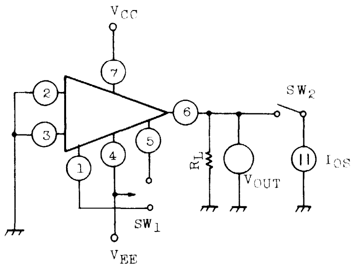
CMV_{IN} : $V_{OUT}=\pm10(V_{DC})$, V_{IN} MEASURED

CMRR : $V_{IN}=7.07(V_{rms})$, V_{OUT} MEASURED

$$CMRR = 20 \log \frac{V_{IN}}{\frac{V_{OUT}}{1000}} = 20 \log \frac{7070}{V_{OUT}} \text{ (dB)}$$

TA7504P, TA7504S

(4) V_{OM}, V_{OMR}, I_{OS}



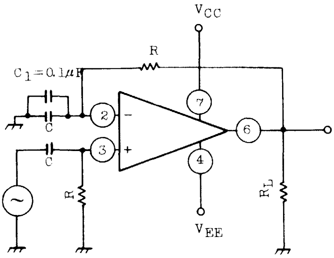
V_{OM}, V_{OMR} : SW_2 : OPEN CIRCUIT

SW_1 : TERMINAL 1 OR 5

I_{OS} : SW_2 : SHORT CIRCUIT

SW_1 : TERMINAL 1 OR 5

(5) G_V, V_{Op-p}



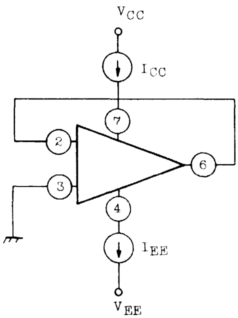
C : DC COUPLE

C_I : HF BYPASS

$\omega \gg 1/RC$

$G_V = V_{OUT}/V_{IN}$

(6) P_D

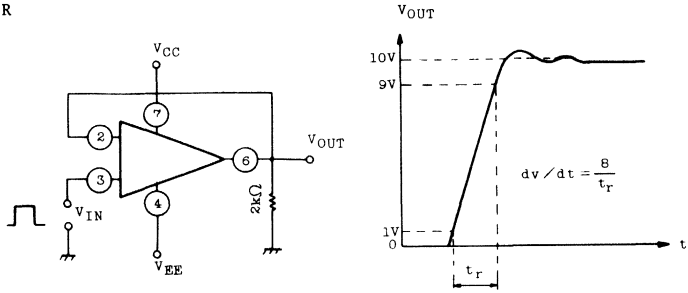


$P_D = (V_{CC} - V_{EE})\ I_{CC}$

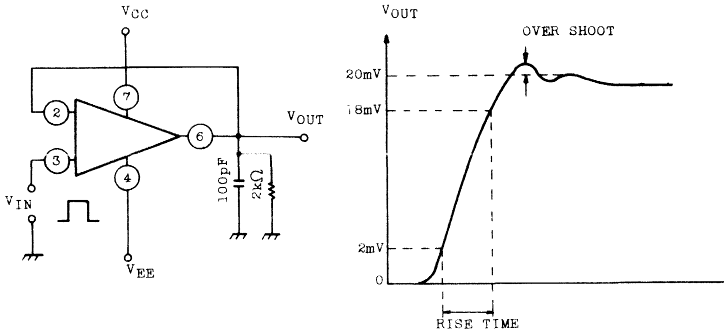
$= (V_{CC} - V_{EE})\ I_{EE}$

TA7504P, TA7504S

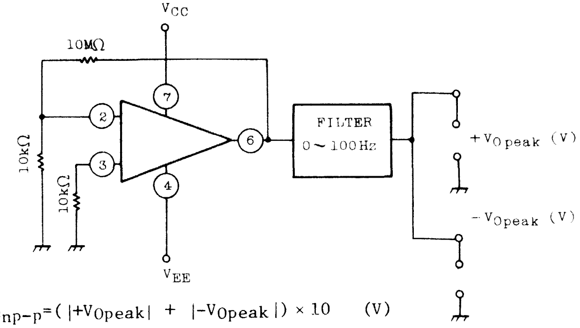
(7) SR



(8) RESPONSE TIME

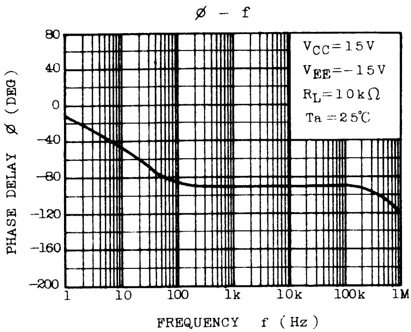


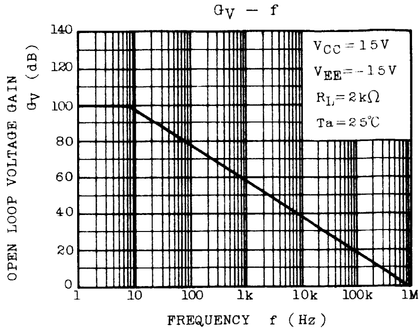
(9) e_{np-p}

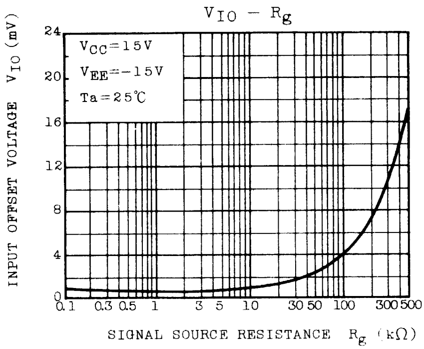


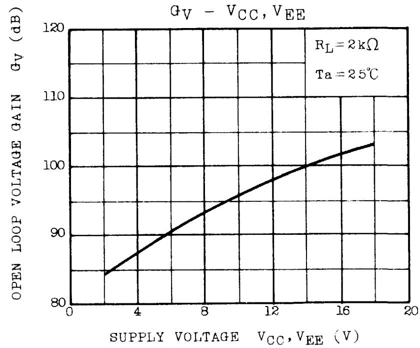
$e_{np-p} = (|+V_{O peak}| + |-V_{O peak}|) \times 10$ (V)

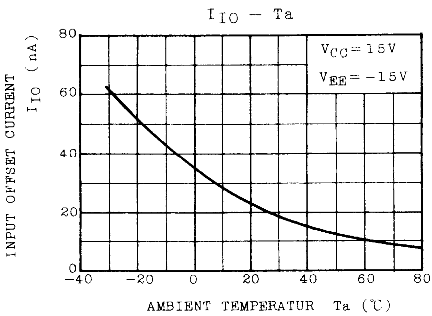
TA7504P, TA7504S

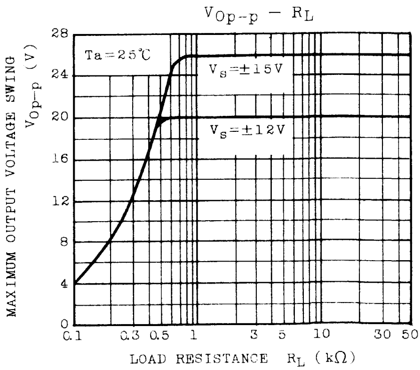




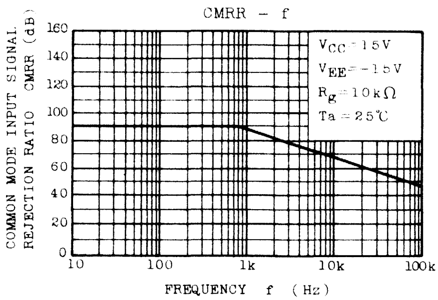


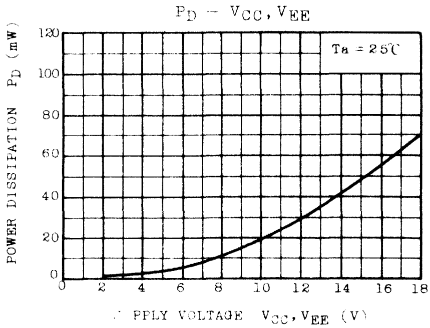


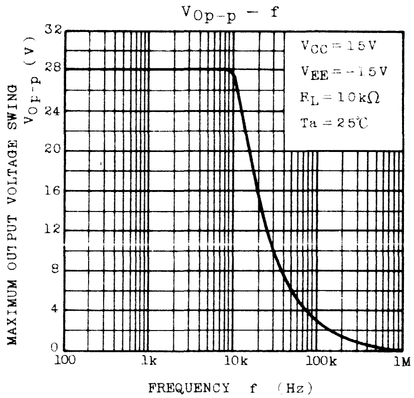


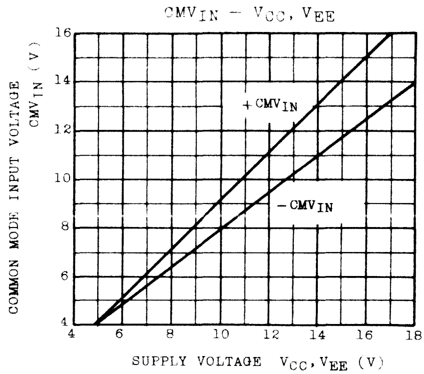


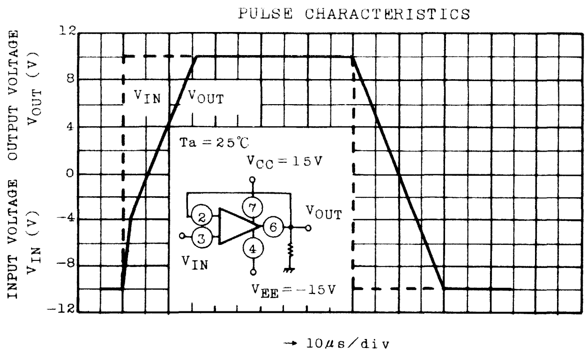
TA7504P, TA7504S











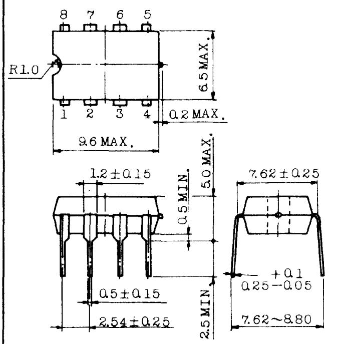
TA7506P

BIPOLAR LINEAR INTEGRATED CIRCUIT
SILICON MONOLITHIC

SINGLE OPERATIONAL AMPLIFIER
OPERATIONAL AMPLIFIER
DC AMPLIFIER

- High Gain
- High Input Resistance
- High Differential Input Voltage
- Wide Common Mode Input Voltage Range
- Absence of Latch-up
- Offset Null Capability
- Short Circuit Protection
- Feed Forward Compensation

INDUSTRIAL APPLICATION
Unit in mm

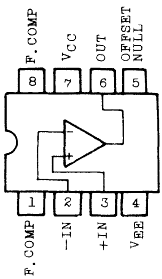


JEDEC	—
TOSHIBA	5−10C

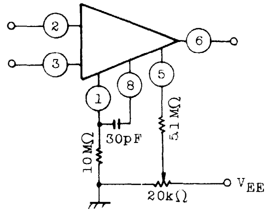
MAXIMUM RATINGS (Ta=25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}, V_{EE}	±18	V
Differential Input Voltage	DV_{IN}	±30	V
Input Voltage	V_{IN}	$V_{CC} \sim V_{EE}$	V
Power Dissipation	P_D	300	mW
Operating Temperature	Topr	-30 ~ 75	°C
Storage Temperature	Tstg	-55 ~ 125	°C

PIN CONNECTION
(TOP VIEW)



VOLTAGE OFFSET NULL CAPABILITY



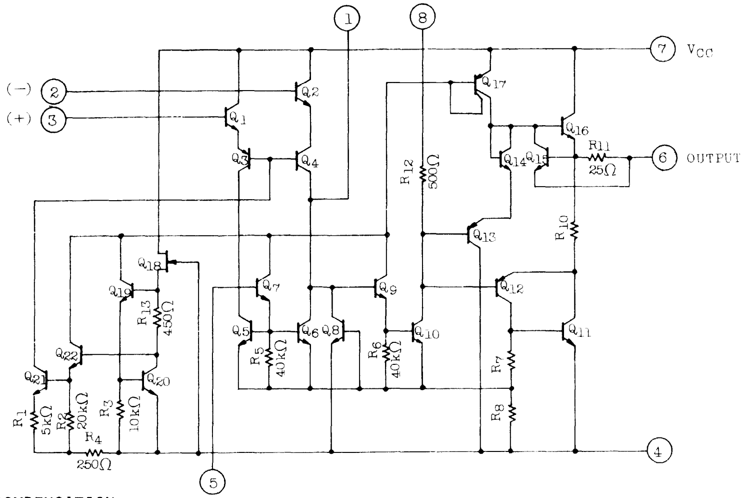
TA7506P

ELECTRICAL CHARACTERISTICS (V_{CC}, V_{EE}=±5~±15V, Ta=25°C)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	V_{IO}	1	$R_g \leqq 50k\Omega$	-	-	5	mV
Input Offset Current	I_{IO}	2	-	-	2	50	nA
Input Bias Current	I_I	2	-	-	50	250	nA
Common Mode Input Voltage	CMV_{IN}	3	-	±12	-	-	V
Maximum Output Voltage	V_{OM}	4	$R_L \geqq 10k\Omega$, V_{CC}=15V	±12	±14	-	V
	V_{OMR}	4	$R_L \geqq 2k\Omega$, V_{EE}=-15V	±10	±13	-	V
Maximum Output Voltage Swing	V_{Op-p}	5	$R_L \geqq 10k\Omega$, f=1kHz	24	28	-	V
Output Short Circuit Current	I_{OS}	4	-	-	25	-	mA
Input Impedance	Z_{IN}	-	f=1kHz	0.5	2	-	MΩ
Voltage Gain	G_V	5	V_{CC}=15V, V_{EE}=-15V $R_L \geqq 2k\Omega$	25	180	-	$\times 10^3$
Common Mode Input Signal Rejection Ratio	CMRR	3	$R_g \leqq 50k\Omega$	70	90	-	dB
Supply Voltage Rejection Ratio	SVRR	1	$R_g \leqq 50k\Omega$	70	90	-	dB
Supply Current	I_{CC}, I_{EE}	-	V_{CC}=15V, V_{EE}=-15V	-	1.8	3	mA
Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	1	$R_g \leqq 50k\Omega$	-	-	30	μV/°C
Temperature Coefficient of Input Offset Current	$\Delta I_{IO}/\Delta T$			-	-	-0.6	nA/°C

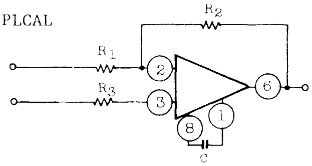
TA7506P

EQUIVALENT CIRCUIT

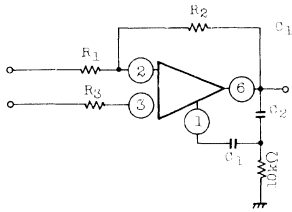


FREQUENCY COMPENSATION CIRCUIT

I. TYPLCAL



II. TWO POLE

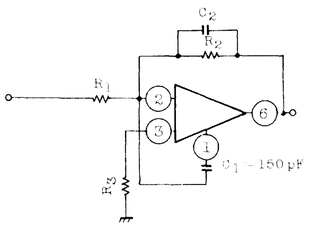


$C_1 \geq \frac{R_1}{R_1 + R_2} \cdot C_s$

$C_2 = 10C_1$

$C_s = 30\,pF$

III. FEED FORWARD



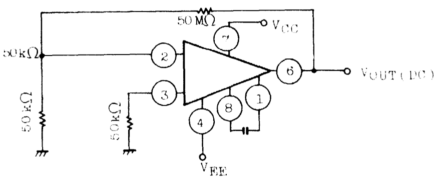
$C_2 = \frac{1}{2\pi f_0 R_2}$

$f_0 \doteqdot 3MHz$

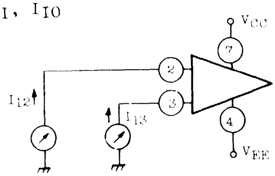
TA7506P

TEST CIRCUIT

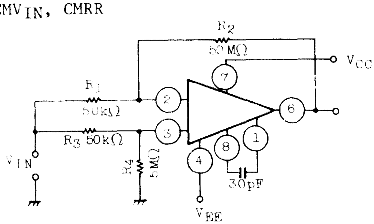
(1) V_{IO}, $\Delta V_{IO}/\Delta T$, SVRR



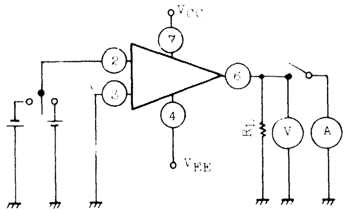
(2) I_I, I_{IO}



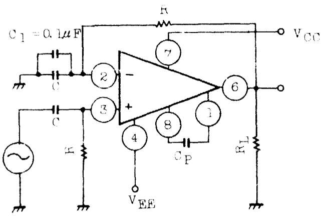
(3) CMV_{IN}, CMRR



(4) V_{OM}, V_{OMR}, I_{OS}



(5) G_V, V_{Op-p}



Cp : FREQUENCY COMPENSATION

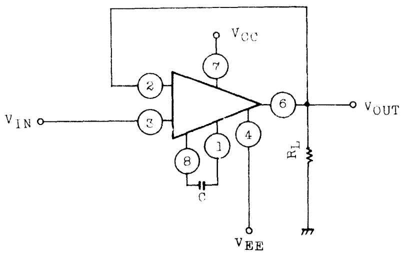
C : COUPLING CONDENSER

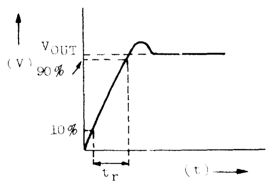
C_I : HIGH FREQUENCY CONDENSER

$\omega \gg 1/RC$

$G_V = V_{OUT}/V_{IN}$

(6) PULSE RESPONSE

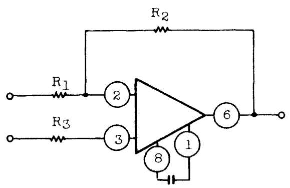


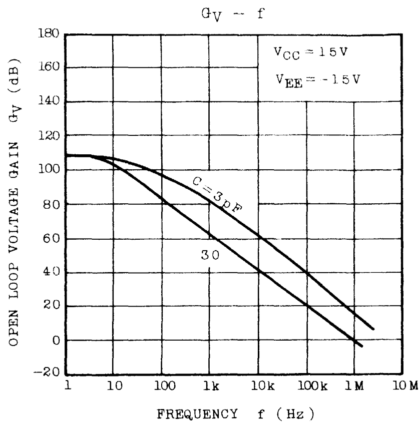


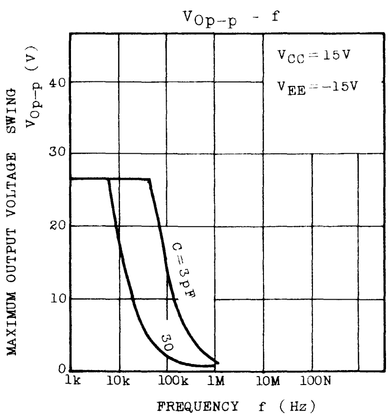
$dv/dt = \frac{1}{tr} \cdot V_{OUT} \times 0.8 (V/\mu s)$

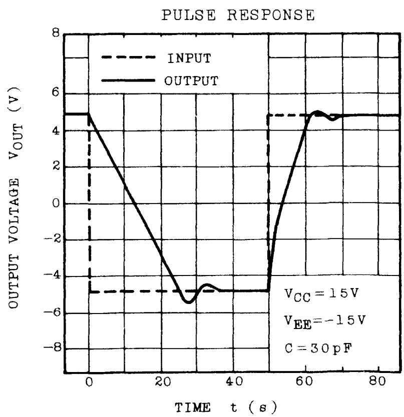
TA7506P

TYPLCAL AMPLIFIER CIRCUIT I



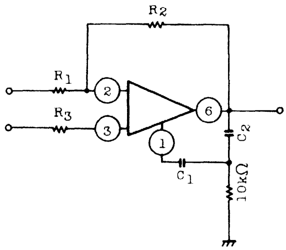


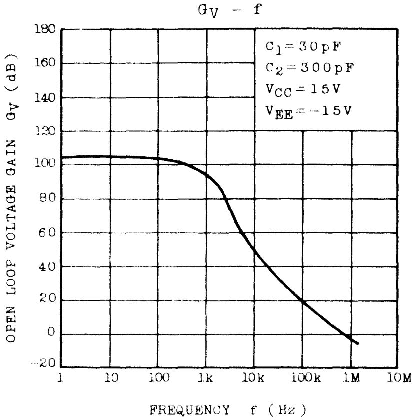


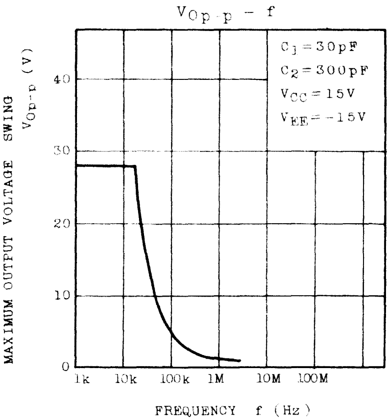


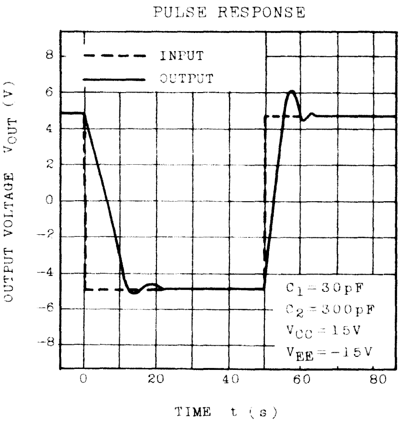
TA7506P

TYPICAL AMPLIFIER CIRCUIT II



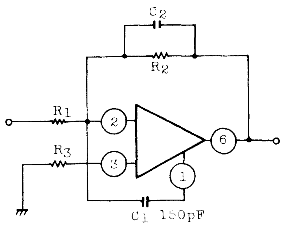


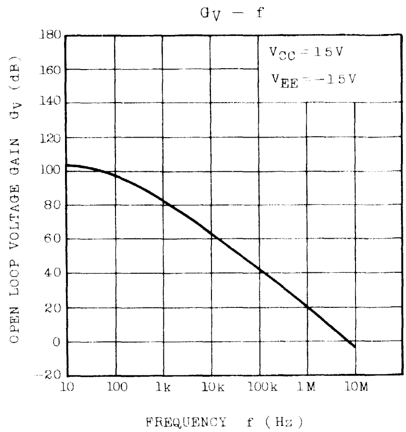


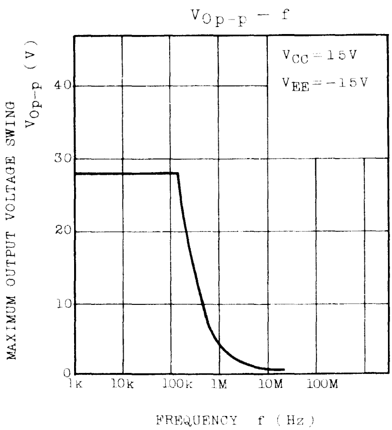


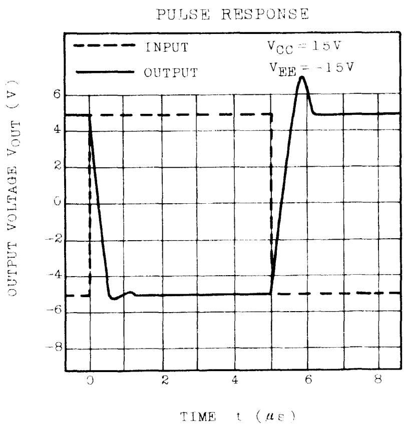
TA7506P

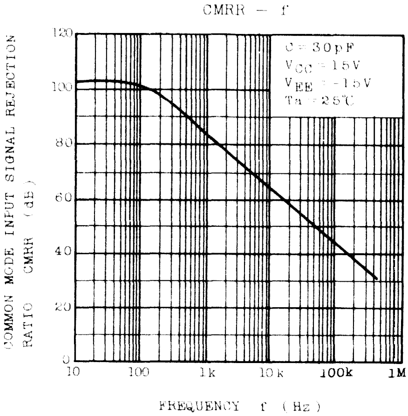
TYPICAL AMPLIFIER CIRCUIT Ⅲ

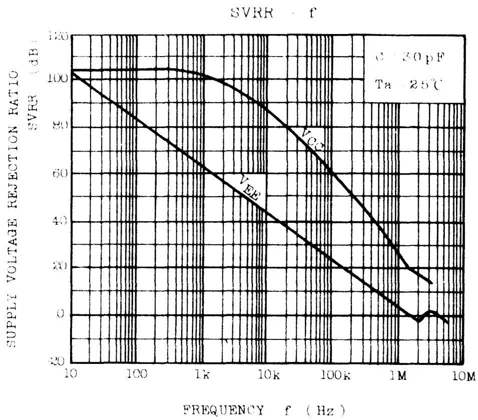


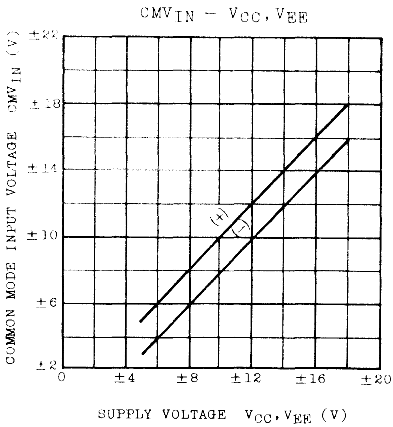


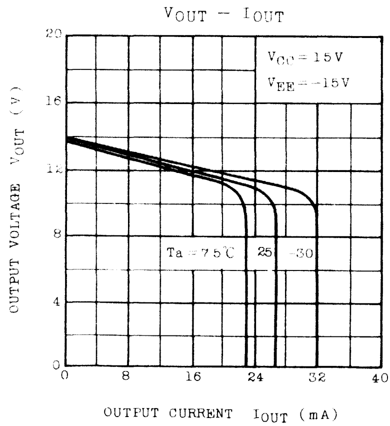




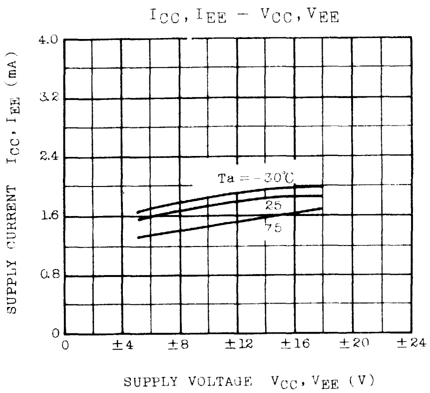

CMRR − f
C = 30pF
V_{CC} = 15V
V_{EE} = −15V
Ta = 25°C
COMMON MODE INPUT SIGNAL REJECTION RATIO CMRR (dB)
FREQUENCY f (Hz)
0
20
40
60
80
100
120
10
100
1k
10k
100k
1M


SVRR − f
C = 30pF
Ta = 25°C
V_{CC}
V_{EE}
SUPPLY VOLTAGE REJECTION RATIO SVRR (dB)
FREQUENCY f (Hz)
-20
0
20
40
60
80
100
120
10
100
1k
10k
100k
1M
10M

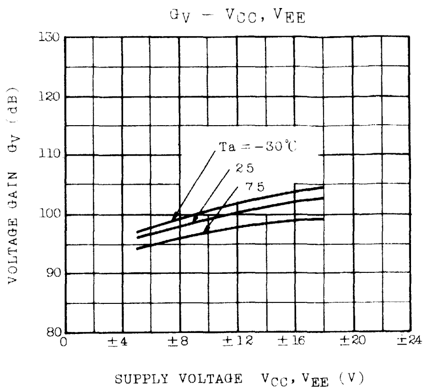

CMV_{IN} − V_{CC}, V_{EE}
(+)
(−)
COMMON MODE INPUT VOLTAGE CMV_{IN} (V)
SUPPLY VOLTAGE V_{CC}, V_{EE} (V)
±2
±6
±10
±14
±18
±22
0
±4
±8
±12
±16
±20


V_{OUT} − I_{OUT}
V_{CC} = 15V
V_{EE} = −15V
Ta = 75°C
25
−30
OUTPUT VOLTAGE V_{OUT} (V)
OUTPUT CURRENT I_{OUT} (mA)
0
4
8
12
16
20
0
8
16
24
32
40

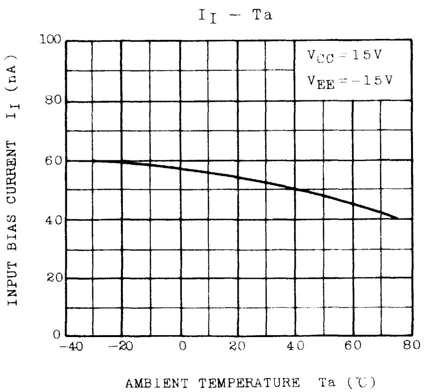
TA7506P



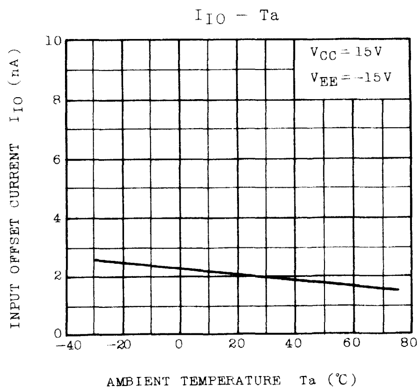
$I_{CC}, I_{EE} - V_{CC}, V_{EE}$
SUPPLY CURRENT I_{CC}, I_{EE} (mA)
4.0
3.2
2.4
1.6
0.8
0
Ta = −30°C
25
75
±4
±8
±12
±16
±20
±24
SUPPLY VOLTAGE V_{CC}, V_{EE} (V)



$G_V - V_{CC}, V_{EE}$
VOLTAGE GAIN G_V (dB)
130
120
110
100
90
80
Ta = −30°C
25
75
±4
±8
±12
±16
±20
±24
SUPPLY VOLTAGE V_{CC}, V_{EE} (V)



$I_I - Ta$
INPUT BIAS CURRENT I_I (nA)
100
80
60
40
20
0
V_{CC} = 15V
V_{EE} = −15V
−40
−20
0
20
40
60
80
AMBIENT TEMPERATURE Ta (°C)



$I_{IO} - Ta$
INPUT OFFSET CURRENT I_{IO} (nA)
10
8
6
4
2
0
V_{CC} = 15V
V_{EE} = −15V
−40
−20
0
20
40
60
80
AMBIENT TEMPERATURE Ta (°C)

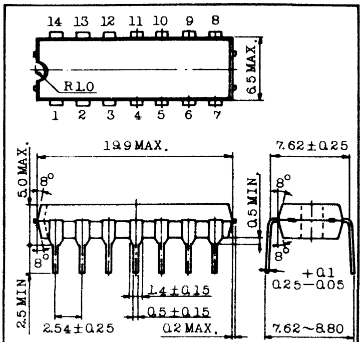
BIPOLAR LINEAR INTEGRATED CIRCUIT
SILICON MONOLITHIC

TA7521P

DUAL COMPARATOR
VOLTAGE COMPARATOR

- Tow Circuits/Package
- Possible to operate at +3V Single Supply
- Possible to gain Inverted Output
- Large Common Mode Voltage Range
- Absence of Latch-Up

Unit in mm



Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.14 leads.

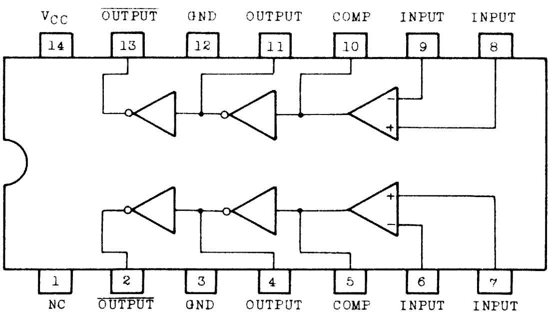
JEDEC	—
TOSHIBA	5−21D

MAXIMUM RATINGS (Ta=25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	18	V
Power Dissipation	P_D	300	mW
Differential Input Voltage	DV_{IN}	±18	V
Common Mode Input Voltage	CMV_{IN}	$+V_{CC}\sim -5$	V
Sink Current	I_{sink}	20	mA
Operating Temperature	T_{opr}	$-40\sim 85$	°C
Storage Temperature	T_{stg}	$-55\sim 125$	°C

PIN CONNECTION (TOP VIEW)

COMP : FREQUENCY COMPENSATION TERMINAL



TA7521P

RECOMMENDED CONDITION

Supply Voltage	5 ~ 12	V
Common Mode Input Voltage	1 ~ (V_{CC}-0.5)	V
Sink Current	10	mA

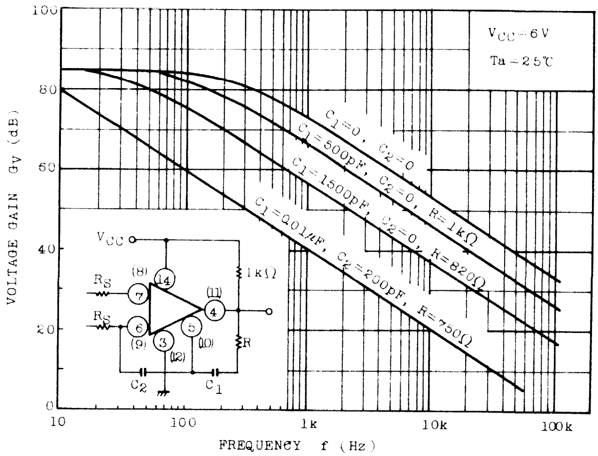
ELECTRICAL CHARACTERISTICS (V_{CC}=6V, Ta=25°C)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage		V_{IO}	-	$R_S \leq 100\Omega$	-	1	5	mV
Input Offset Current		I_{IO}	-	-	-	15	50	nA
Input Bias Current		I_I	-	-	-	120	300	nA
Voltage Gain		$G_{\overline{V}}$	-	$R_L \geqq 1k\Omega$, f=100Hz	75	85	-	dB
		G_V^+	-	$R_L \geqq 1k\Omega$, f=100Hz	80	95	-	dB
Output Voltage	"H" Level	V_{OH}	-	I_{OH}=-2mA	4.6	5.1	-	V
	"L" Level	V_{OL}	-	I_{OL}=10mA	-	0.2	0.4	V
Common Mode Input Voltage	"H" Level	$CMV_{IN(H)}$	-	-	5.8	5.9	-	V
	"L" Level	$CMV_{IN(L)}$	-	-	-	0.8	0.9	V
Common Mode Input Signal Rejection Ratio		CMRR	-	f=100Hz	80	90	-	dB
Power Dissipation		P_D	-	-	-	15	25	mW

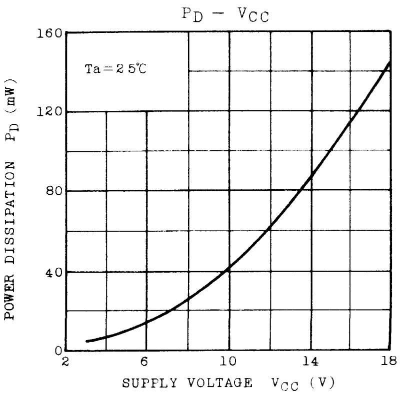
Note: $G_{\overline{V}}$: Inverted output voltage gain.

TA7521P

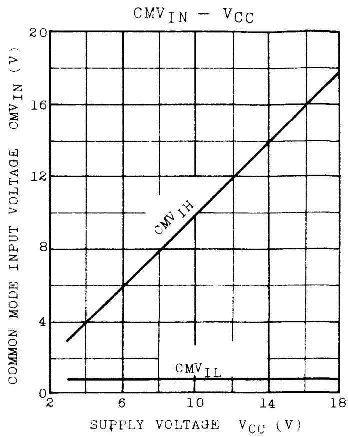
FREQUENCY CHARACTERISTICS OF OPEN LOOP GAIN



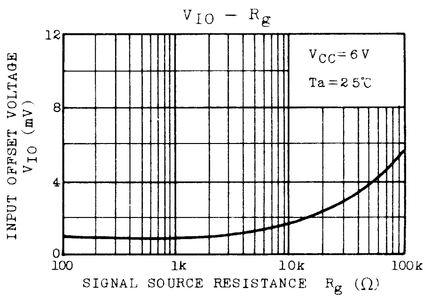
TA7521P



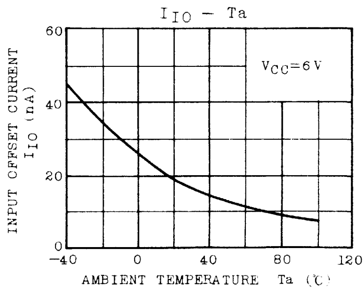
$P_D - V_{CC}$
Ta = 25°C
POWER DISSIPATION P_D (mW)
SUPPLY VOLTAGE V_{CC} (V)
160
120
80
40
0
2
6
10
14
18



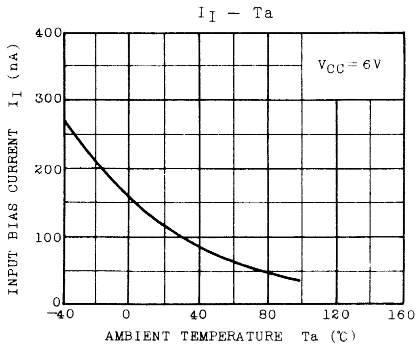
$CMV_{IN} - V_{CC}$
COMMON MODE INPUT VOLTAGE CMV_{IN} (V)
SUPPLY VOLTAGE V_{CC} (V)
CMV_{IH}
CMV_{IL}
20
16
12
8
4
0
2
6
10
14
18



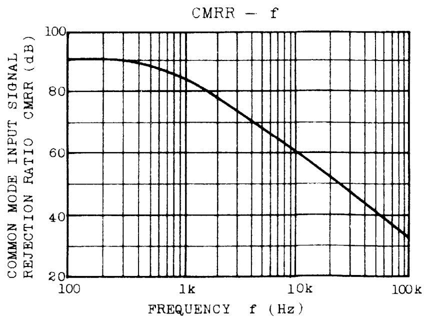
$V_{IO} - R_g$
V_{CC} = 6 V
Ta = 25°C
INPUT OFFSET VOLTAGE V_{IO} (mV)
SIGNAL SOURCE RESISTANCE R_g (Ω)
12
8
4
0
100
1k
10k
100k



$I_{IO} - Ta$
V_{CC} = 6 V
INPUT OFFSET CURRENT I_{IO} (nA)
AMBIENT TEMPERATURE Ta (°C)
60
40
20
0
−40
0
40
80
120



$I_I - Ta$
V_{CC} = 6 V
INPUT BIAS CURRENT I_I (nA)
AMBIENT TEMPERATURE Ta (°C)
400
300
200
100
0
−40
0
40
80
120
160



CMRR − f
COMMON MODE INPUT SIGNAL REJECTION RATIO CMRR (dB)
FREQUENCY f (Hz)
100
80
60
40
20
100
1k
10k
100k

BIPOLAR LINEAR INTEGRATED CIRCUIT
SILICON MONOLITHIC

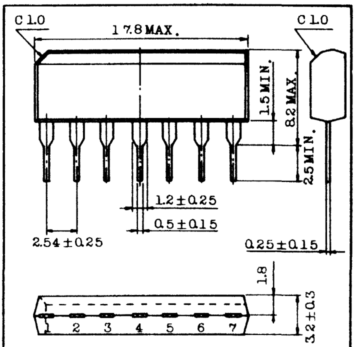
TA7523S

SINGLE COMPARATOR.

COMMUNICATION AND INDUSTRIAL USE

- Be Possible to Operate at the Wide Range Single or Two Supply Voltage.
- Output is Open Collector and Wired-OR Possible.
- Wide Common Mode Input Voltage : $0V \sim V_{CC}-1.5V_{DC}$
- Output is Compatible with TTL and CMOS.
- Wide Supply Voltage Range
  : $2V_{DC} \sim 36V_{DC}$ or $\pm 1V_{DC} \sim \pm 18V_{DC}$
- With Two Output Terminals (OUT, $\overline{\text{OUT}}$)
- Hysterisis Voltage Width is Variable by External Resistor.

Unit in mm



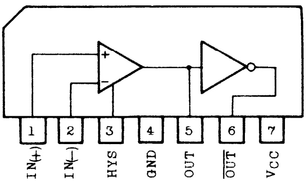
Lead pitch is 2.54 and torelance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 lead.

JEDEC	―
TOSHIBA	5−18A

MAXIMUM RATINGS (Ta=25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	±18 or 36	V
Differential Input Voltage	DV_{IN}	±36	V
Common Mode Input Voltage	CMV_{IN}	$-0.3 \sim V_{CC}$	V
Power Dissipation	P_D	500	mW
Operating Temperature	Topr	$-40 \sim 85$	°C
Storage Temperature	Tstg	$-55 \sim 125$	°C

PIN CONNECTION

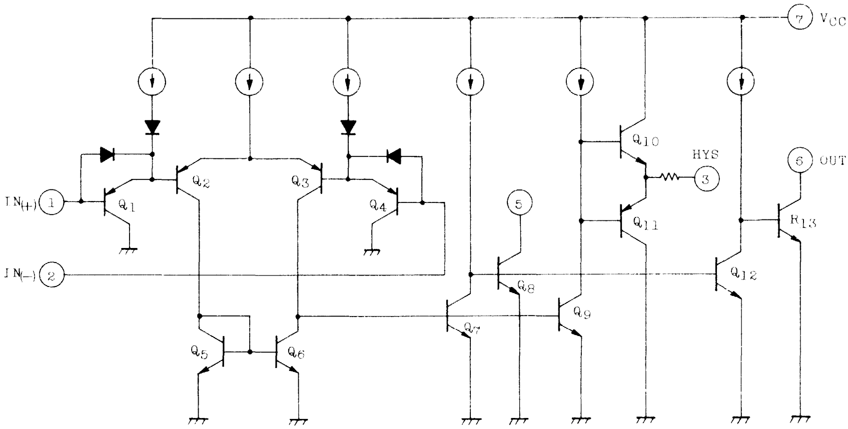


TA7523S

ELECTRICAL CHARACTERISTICS (V_{CC}=5V, Ta=25°C)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	V_{IO}	4	V_O=1.4V	-	3	7	mV
Input Bias Current	I_I	2	-	-	25	250	nA
Input Offset Current	I_{IO}	2	-	-	5	50	nA
Common Mode Input Voltage	CMV_{IN}	4	-	0	-	V_{CC} -1.5	V
Voltage Gain	G_V	-	R_L=15kΩ	-	200	-	V/mV
Supply Current	I_{CC}	1	No Load	-	0.5	3	mA
Sink Current	I_{SINK}	5	$IN_{(+)}$=0V, $IN_{(-)}$=1V, V_{OL}=1.5V	6	16	-	mA
Output Voltage	V_{OL}	5	$IN_{(+)}$=0V, $IN_{(-)}$=1V, I_{SINK}=3mA	-	0.2	0.4	V
Output Leak Current	I_{LEAK}	3	$IN_{(+)}$=0V, $IN_{(-)}$=0V, V_O=5V	-	0.1	-	nA
Response Time	t_{rsp}	6	R_L=5.1kΩ, C_L=15pF	-	1.3	-	μs

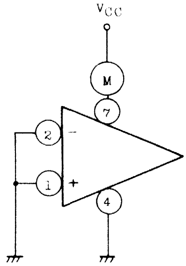
EQUIVALENT CIRCUIT



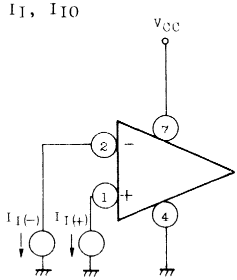
TA7523S

TEST CIRCUIT

(1) I_{CC}

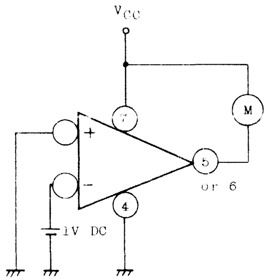


(2) I_I, I_{IO}

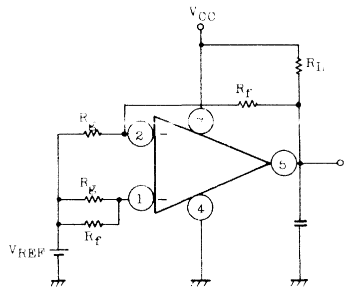


$I_{IO}=I_{I(+)}-I_{I(-)}$

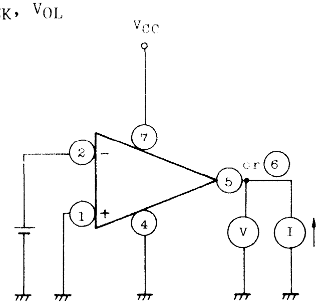
(3) I_{LEAK}



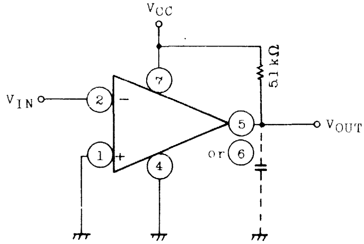
(4) V_{IO}, CMV_{IN}



(5) I_{SINK}, V_{OL}



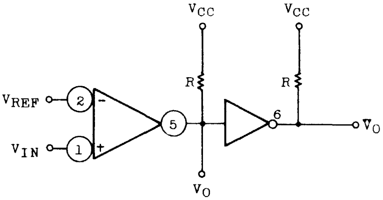
(6) t_{rsp}



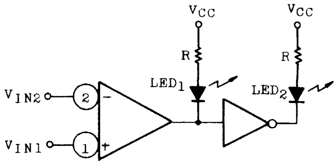
TA7523S

APPLICATION CIRCUIT

1. GENERAL COMPARATOR



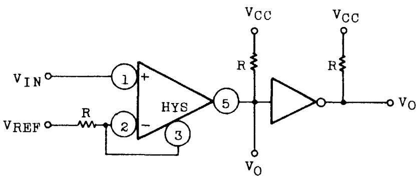
2. COMPARE WITH INPUT VOLTAGE

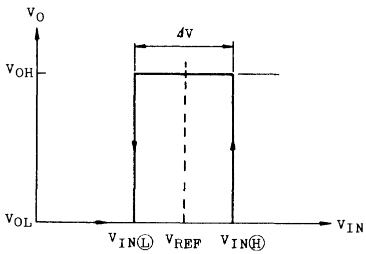


LED 2 IS LIGHTED AT $V_{IN1} > V_{IN2}$

LED 1 IS LIGHTED AT $V_{IN1} < V_{IN2}$

3. COMPARATOR WITH HYSTERESIS





V_{OH} : OUTPUT VOLTAGE ("H" LEVEL)

V_{OL} : OUTPUT VOLTAGE ("L" LEVEL)

V_{IN} (H) :
TURNOVER INPUT VOLTAGE ("H" LEVEL)

V_{IN} (L) :
TURNOVER INPUT VOLTAGE ("L" LEVEL)

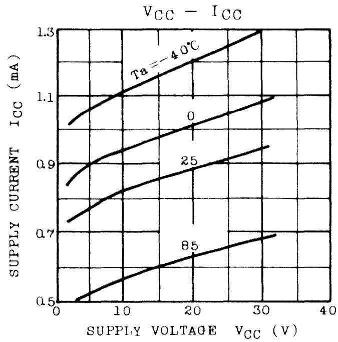
V_{REF} : REFERENCE VOLTAGE

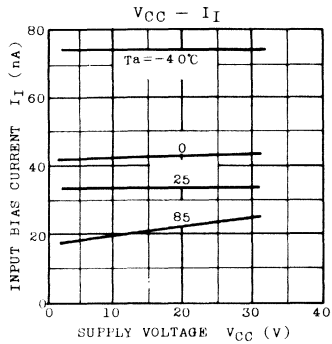
ΔV : HYSTERESIS WIDTH

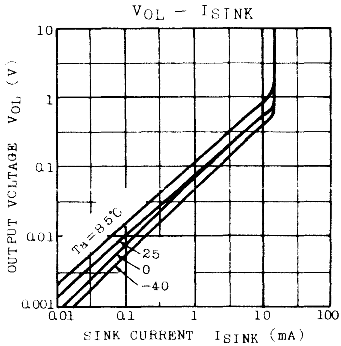
Calculate the Hysterisis width using the following equation

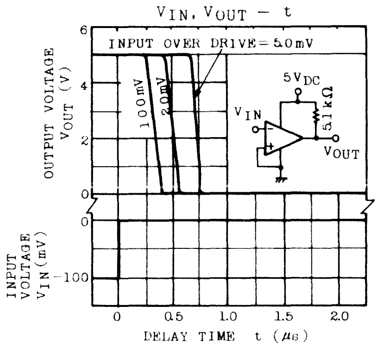
: $\Delta V \doteqdot (V_{CC}-2)\dfrac{R}{R+10}$ $\quad V_{CC}(V)\ R\ (k\Omega)$

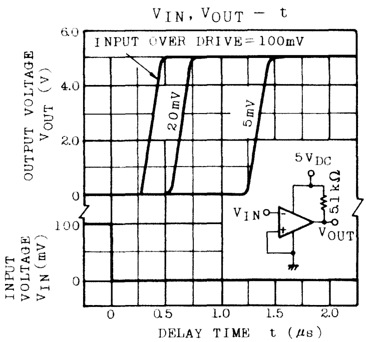
TA7523S


VCC − ICC
SUPPLY CURRENT ICC (mA)
SUPPLY VOLTAGE VCC (V)
Ta=−40℃
0
25
85
1.3
1.1
0.9
0.7
0.5
0
10
20
30
40


VCC − II
INPUT BIAS CURRENT II (nA)
SUPPLY VOLTAGE VCC (V)
Ta=−40℃
0
25
85
80
60
40
20
0
10
20
30
40


VOL − ISINK
OUTPUT VOLTAGE VOL (V)
SINK CURRENT ISINK (mA)
Ta=85℃
25
0
−40
10
1
0.1
0.01
0.001
0.01
0.1
1
10
100


VIN, VOUT − t
INPUT OVER DRIVE=50mV
100mV
20mV
5VDC
5.1kΩ
VIN
VOUT
OUTPUT VOLTAGE VOUT (V)
INPUT VOLTAGE VIN (mV)
DELAY TIME t (μs)
6
4
2
0
0
−100
0
0.5
1.0
1.5
2.0

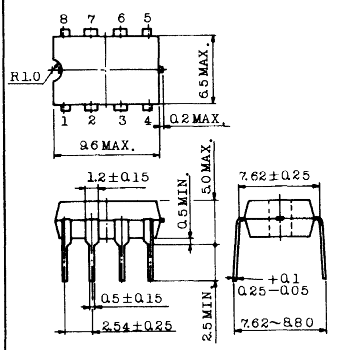

VIN, VOUT − t
INPUT OVER DRIVE=100mV
20mV
5mV
5VDC
5.1kΩ
VIN
VOUT
OUTPUT VOLTAGE VOUT (V)
INPUT VOLTAGE VIN (mV)
DELAY TIME t (μs)
6.0
4.0
2.0
0
100
0
0
0.5
1.0
1.5
2.0

TA7555P

BIPOLAR LINEAR INTEGRATED CIRCUIT
SILICON MONOLITHIC

TIMER APPLICATIONS

Unit in mm



JEDEC	—
TOSHIBA	5−10C

DESCRIPTION

The TA7555P monolithic circuit is a highly stable device as producing accurate time delay or timing pulse.

Additional terminals are provided for triggering or reseting, if desired.

In the time delay or monostable mode of operation, the time is precisely controlled by one external resistor and capacitor.

In the astable mode of operation, the frequency and duty cycle are accurately and independently controlled with two external resistors and one capacitor.

The circuit of the TA7555P may be triggered and reset on falling waveforms, and the output structure can source and sink up to 200mA or drive TTL circuit. Operation is specified for supplies of 5 to 15 volts.

FEATURES

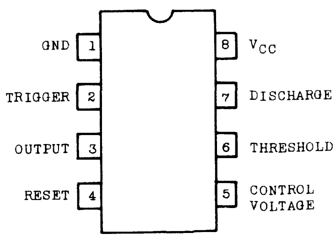
. Timing from microseconds through hours
. Operates in both astable and monostable modes
. Adjustable duty cycle
. Output can souce or sink 200mA
. Output TTL compatible
. Temperature stability of 0.005%/°C (Typ.)
. Normally ON or normally OFF output
. Direct replacement for SE555/NE555

MAXIMUM RATINGS (Ta=25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	18	V
Power Dissipation	P_D	600	mW
Operating Temperature	Topr	-30 ~ 75	°C
Storage Temperature	Tstg	-55 ~ 125	°C

PIN CONNECTION

(TOP VIEW)



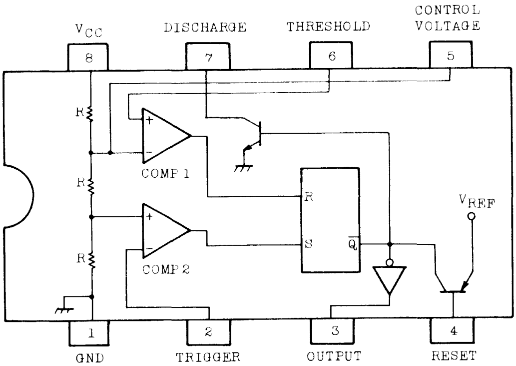
TA7555P

ELECTRICAL CHARACTERISTICS ($Ta=25^\circ C$, $V_{CC}=5V \sim 15V$)

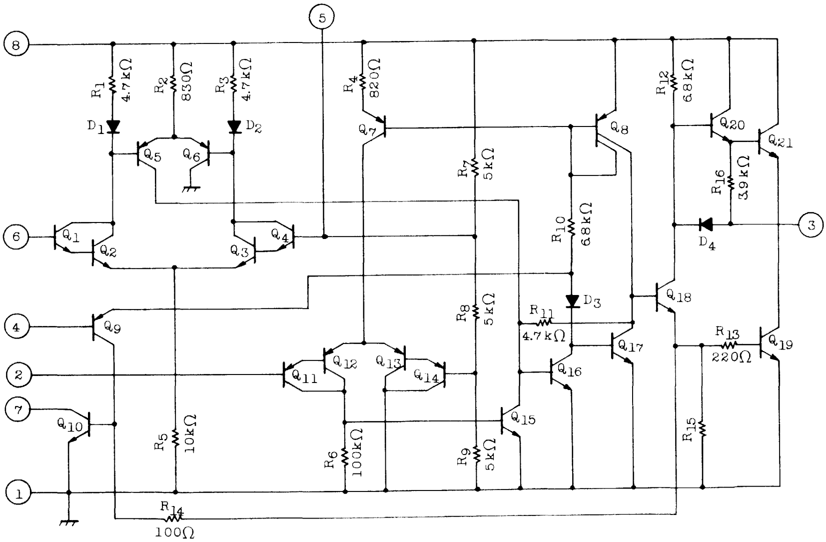
CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}	-	-		4.5	-	16	V
Supply Current	I_{CC}	-	V_{CC}=5V, $R_L=\infty$ Low State		-	3	6	mA
			V_{CC}=15V, $R_L=\infty$ Low State		-	10	15	
Control Voltage	V_{CT}	-	V_{CC}=5V		2.6	3.33	4	V
			V_{CC}=15V		9	10	11	
Threshold Voltage	V_{TH}	-	-		-	(2/3) V_{CC}	-	V
Threshold Current	I_{TH}	-	V_{CC}=5V, 15V		-	0.1	0.25	μA
Trigger Voltage	V_{TG}	-	V_{CC}=5V		-	1.67	-	V
			V_{CC}=15V		-	5	-	
Trigger Current	I_{TG}	-	-		-	0.5	-	μA
Reset Voltage	V_{RT}	-	-		0.4	0.7	1.0	V
Reset Current	I_{RT}	-	-		-	0.1	-	mA
Initial Accuracy	-	-	MONOSTABLE MODE R_A, R_B=1kΩ~100kΩ C=0.1μF, V_{CC}=15V		-	1	-	%
Drift with Temperature					-	50	-	ppm/°C
Drift with Supply Voltage					-	0.1	-	%/V
Output Voltage ("L" Level)	V_{OL}	-	V_{CC}=15V	I_{sink}=10mA	-	0.1	0.25	V
				I_{sink}=50mA	-	0.4	0.75	
				I_{sink}=100mA	·	2	2.5	
				I_{sink}=200mA	-	2.5	-	
			V_{CC}=5V	I_{sink}=5mA	-	0.25	0.35	
				I_{sink}=8mA	-	-	-	
Output Voltage ("H" Level)	V_{OH}	-	V_{CC}=15V	I_{source}=100mA	12.75	13.3	-	V
				I_{source}=200mA	-	12.5	-	
			V_{CC}=5V	I_{source}=100mA	2.75	3.3	-	
Rise Time	T_r	-	-		-	100	-	ns
Fall Time	T_f	-			-	100	-	ns

TA7555P

BLOCK DIAGRAM



EQUIVALENT CIRCUIT



APPLICATIONS

- . DC-DC CONVERTER
- . LINEAR RAMP GENERATOR
- . PULSE GENERATOR
- . PRECISION TIMING
- . SEQUENTIAL TIMING
- . TIMING DELAY GENERATION
- . PULSE WIDTH MODULATION
- . PULSE

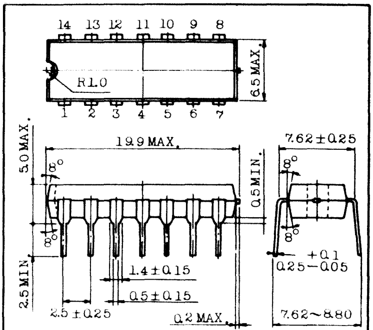
BIPOLAR LINEAR INTEGRATED CIRCUIT
SILICON MONOLITHIC

TA75339P

COMMUNICATION AND INDUSTRIAL USE

VOLTAGE COMPARATORS

Unit in mm



Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.14 leads.

JEDEC	—
TOSHIBA	5−21F

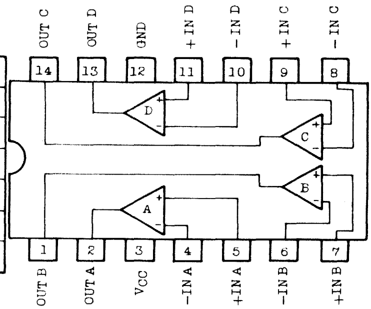
DISCRIPTION

This divice consist of four independent voltage comparators that designed to operate from a single power supply over a wide range of voltage.
Normal Operation from dual supplies is also to be guaranteed on voltage range from 2V to 36V. V_{CC} is necessary at least more 1.5 volts than the input common mode voltage.
The output can be connected to other open collector outputs to achieve Wired-OR relation ship.

FEATURES

. Single Supply Voltage Range or Dual Supplies :
  $2V_{DC}$ to $36V_{DC}$ or $\pm 18V_{DC}$
. Low Supply Current : 0.8mA (Typ.)
. Low Input Offset Voltage: ±2mV (Typ.)
. Wide Input Common Mode Voltage Range: $0V_{DC}$ to V_{CC} - $1.5V_{DC}$
. Output compatible with TTL, DTL, MOS and CMOS Logic System.
. The output can be connected to achieve Wired-OR Relation.

PIN CONNECTION (TOP VIEW)



MAXIMUM RATINGS (Ta=25°C)

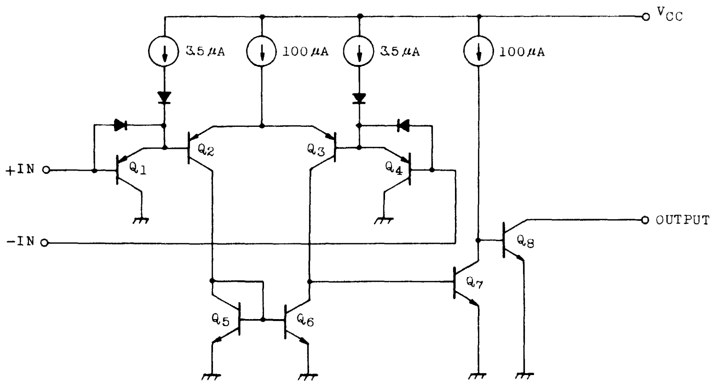
CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	±18 ~ 36	V
Differential Input Voltage	DV_{IN}	±36	V
Common Mode Input Voltage	CMV_{IN}	-0.3 ~ V_{CC}	V
Power Dissipation	P_D	625	mW
Operating Temperature	Topr	-40 ~ 85	°C
Storage Temperature	Tstg	-55 ~ 125	°C

TA75339P

ELECTRICAL CHARACTERISTICS (V_{CC}=5V, Ta=25°C)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	V_{IO}	4	V_O=1.4V	-	2	5	mV
Input Offset Current	I_{IO}	2	-	-	5	50	nA
Input Bias Current	I_I	2	-	-	25	250	nA
Common Mode Input Voltage	CMV_{IN}	4	-	0	-	V_{CC} -1.5	V
Voltage Gain	G_V	-	R_L=15kΩ	-	200	-	V/mV
Supply Current	I_{CC}	1	No Load	-	0.8	2	mA
Sink Current	I_{SINK}	5	+IN=0V, -IN=1V, V_{OL}=1.5V	6	16	-	mA
Output Voltage ("L" Level)	V_{OL}	5	+IN=0V, -IN=1V, I_{SINK}=3mA	-	0.2	0.4	V
Output Leak Current	I_{LEAK}	3	+IN=1V, -IN=0V, V_O=5V	-	0.1	-	nA
Response Time	t_{rsp}	6	R_L=5.1kΩ, C_L=15pF	-	1.3	-	μs

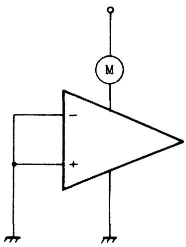
EQUIEVARENT CIRCUIT



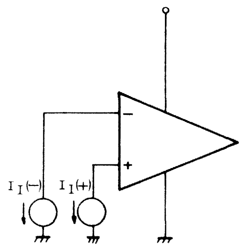
TA75339P

TEST CIRCUIT

(1) I_{CC}

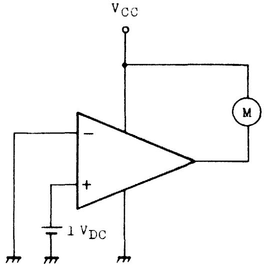


(2) I_I, I_{IO}

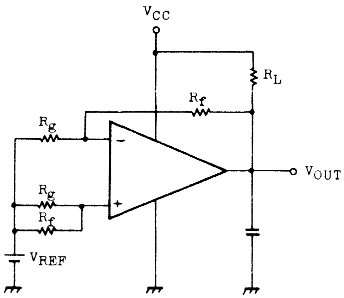


$I_{IO} = I_I(+) - I_I(-)$

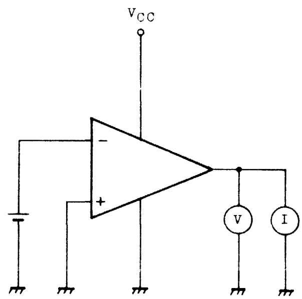
(3) I_{LEAK}



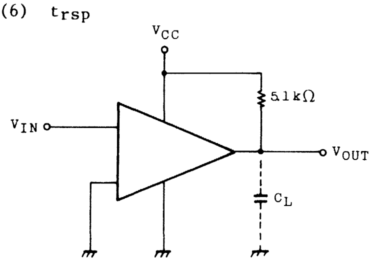
(4) V_{IO}, CMV_{IN}



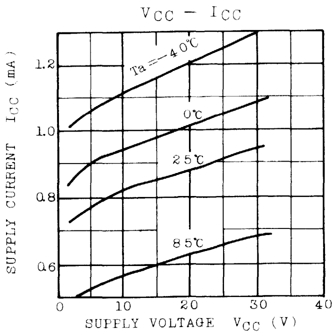
(5) I_{SINK}, V_{OL}

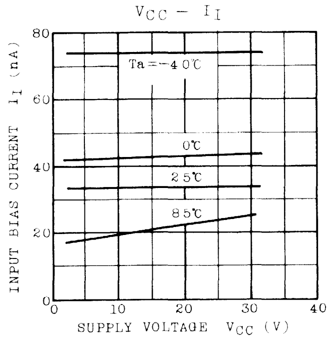


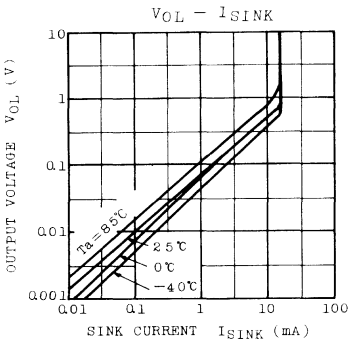
(6) t_{rsp}

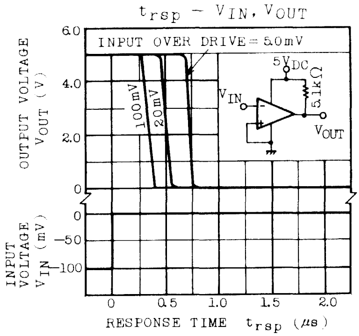


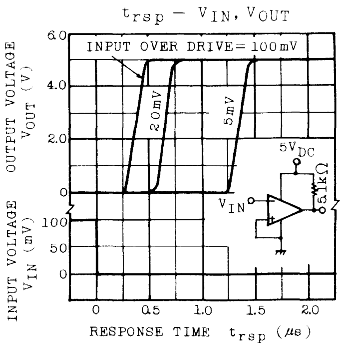
TA75339P


VCC − ICC
SUPPLY CURRENT ICC (mA)
SUPPLY VOLTAGE VCC (V)
Ta=−40℃
0℃
25℃
85℃
1.2
1.0
0.8
0.6
0
10
20
30
40


VCC − II
INPUT BIAS CURRENT II (nA)
SUPPLY VOLTAGE VCC (V)
Ta=−40℃
0℃
25℃
85℃
80
60
40
20
0
10
20
30
40


VOL − ISINK
OUTPUT VOLTAGE VOL (V)
SINK CURRENT ISINK (mA)
Ta=85℃
25℃
0℃
−40℃
10
1
0.1
0.01
0.001
0.01
0.1
1
10
100


trsp − VIN, VOUT
INPUT OVER DRIVE=5.0mV
OUTPUT VOLTAGE VOUT (V)
INPUT VOLTAGE VIN (mV)
100mV
20mV
5VDC
5.1kΩ
VIN
VOUT
6.0
4.0
2.0
0
−50
−100
RESPONSE TIME trsp (μs)
0
0.5
1.0
1.5
2.0


trsp − VIN, VOUT
INPUT OVER DRIVE=100mV
OUTPUT VOLTAGE VOUT (V)
INPUT VOLTAGE VIN (mV)
20mV
5mV
5VDC
5.1kΩ
VIN
6.0
4.0
2.0
0
100
50
RESPONSE TIME trsp (μs)
0
0.5
1.0
1.5
2.0

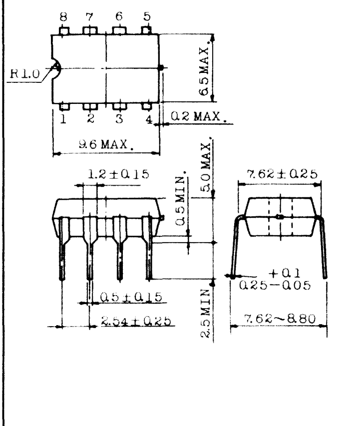
BIPOLAR LINEAR INTEGRATED CIRCUIT
SILICON MONOLITHIC

TA75358P

DUAL OPERATIONAL AMPLIFIER
OPERATIONAL AMPLIFIER
DC AMPLIFIER

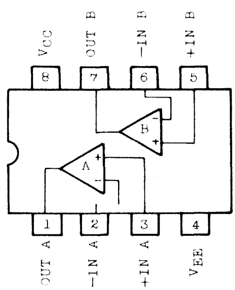
- In the Linear Mode the Input Common Mode Voltage Range Includes Ground
- Two Internally Compensated OP Amps is Single Package
- Low Power Dissipation and Power Drain suitable for Battery Operation
- Differential Input Voltage Range equal to the Power Supply Voltage
- Large Output Voltage Swing ; $0V_{DC}$ to $V_{CC}-1.5V_{DC}$
- Wide Power Supply Voltage Range and Single Power Supply is possible
- Single Supply $3V_{DC}$ to $36V_{DC}$ or Dual Supplies $\pm1.5V_{DC}$ to $18V_{DC}$
- Low Input Biasing Current : $I_I=45nA_{DC}$ (Typ.)

Unit in mm



JEDEC	—
TOSHIBA	5−10C

PIN CONNECTION (TOP VIEW)



MAXIMUM RATINGS (Ta=25°C)

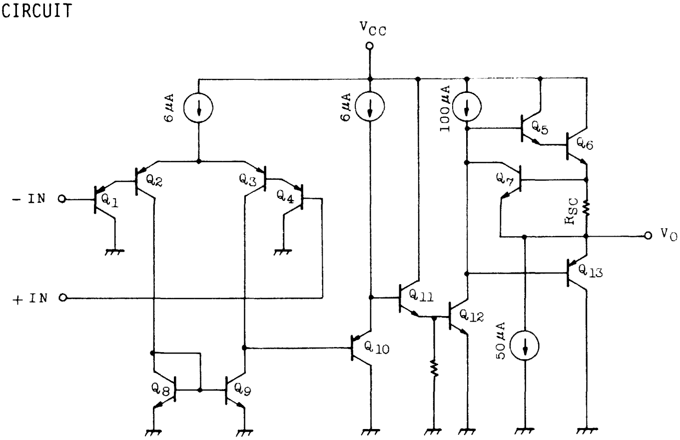
CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}, V_{EE}	±18, 36	V
Differential Input Voltage	DV_{IN}	±36	V
Input Voltage	V_{IN}	-0.3~36	V
Power Dissipation	P_D	500	mV
Operating Temperature	Topr	-40~85	°C
Storage Temperature	Tstg	-55~125	°C

TA75358P

ELECTRICAL CHARACTERISTICS (V_{CC}=5V, V_{EE}=GND, Ta=25°C)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	V_{IO}	1	$R_g \leqq 10k\Omega$	-	2	7	mV
Input Offset Current	I_{IO}	2	-	-	5	50	nA
Input Bias Current	I_I	2	-	-	45	250	nA
Common Mode Input Voltage	CMV_{IN}	3	V_{CC}=30V, V_{EE}=GND	0	-	V_{CC} -1.5	V
Supply Current	I_{CC}, I_{EE}	4	$R_L=\infty$, ALL OP Amps	-	0.7	1.2	mA
Voltage Gain	G_V	5	$R_L \geqq 2k\Omega$	86	100	-	dB
Maximum Output Voltage Swing	V_{OP-p}	6	$R_L=2k\Omega$	0	-	V_{CC} -1.5	V
Common Mode Rejection Ratio	CMRR	3	-	60	85	-	dB
Supply Voltage Rejection Ratio	SVRR	1	$R_g=10k\Omega$	60	100	-	dB
Source Current	I_{source}	6	$-IN=0V_{DC}$, $+IN=1V_{DC}$	20	40	-	mA
Sink Current	I_{sink}	6	$-IN=1V_{DC}$, $+IN=0V_{DC}$	10	20	-	mA

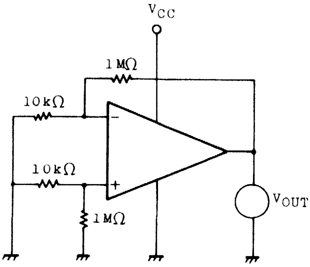
EQUIVALENT CIRCUIT



TA75358P

TEST CIRCUIT

(1) V_{IO}, SVRR



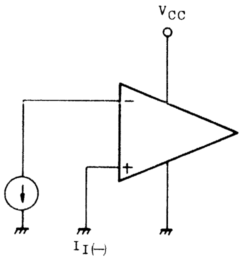
- $V_{IO}=V_{OUT}/100$
- $SVRR=20 \log E$ (dB)

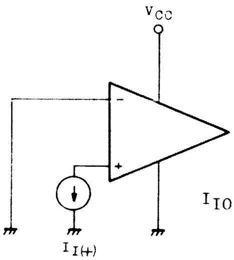
$$E=\left|\frac{V_{OUT1}-V_{OUT2}}{V_{CC1}-V_{CC2}}\right|\times\frac{1}{100}$$

V_{OUT1} : V_{OUT} (V_{CC1}=5V)

V_{OUT2} : V_{OUT} (V_{CC2}=10V)

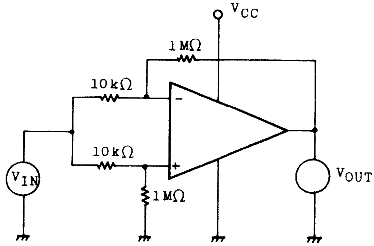
(2) I_I, I_{IO}





$I_{IO}=|I_{I(-)}-I_{I(+)}|$

(3) CMV_{IN}, CMRR



- $CMRR=20 \log G_D/G_C$ (dB)

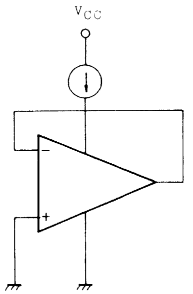
  G_D : DIFFERENTIAL VOLTAGE GAIN

  G_C : COMMON MODE VOLTAGE GAIN

- CMV_{IN} : V_{IN}=0V, V_{CC}-1.5V SUPPLIES

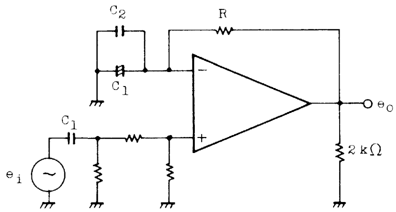
TA75358P

(4) I_{CC}



. I_{CC} : V_{CC}=5V

(5) G_V



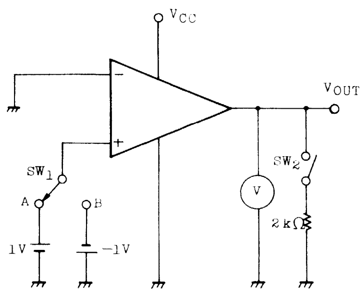
. G_V=20 log e_o/e_i (dB)

R $\geqslant$ $1/W_{C1}$

C_1 : COUPLING CONDENSER

C_2 : HIGH FREQUENCY BYPASS CONDENSER

(6) V_{Op-p}, I_{source}, I_{sink}



. V_{Op-p};

V_{OH} : SW_1 IS SIDE A

V_{OL} : SW_1 IS SIDE B

. I_{source}

SW_1 IS SIDE A

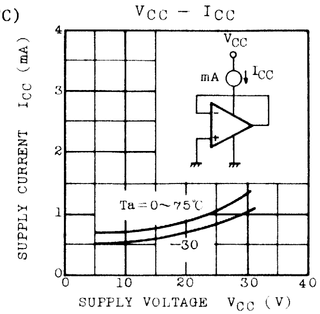
V_{OUT} → 0V MEASURE

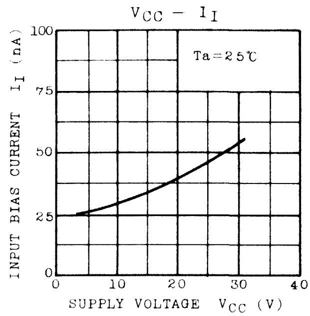
. I_{sink}

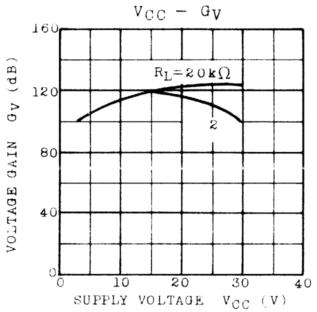
SW_1 IS SIDE B

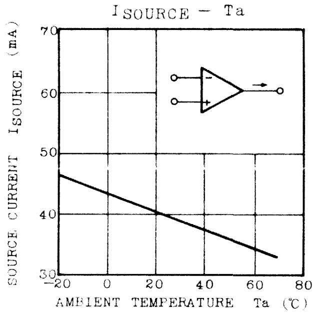
V_{OUT} → 5V MEASURE

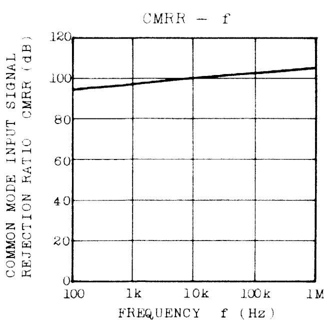
CHARACTERISTICS
(Ta=25°C)

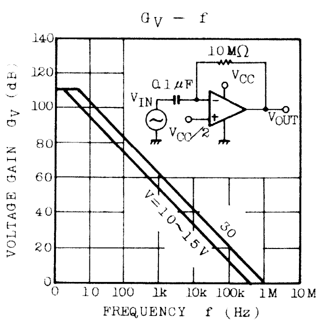




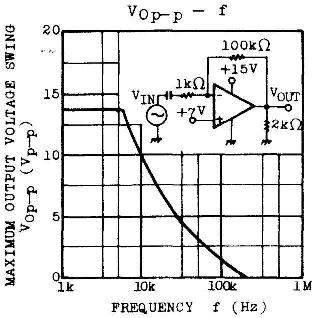


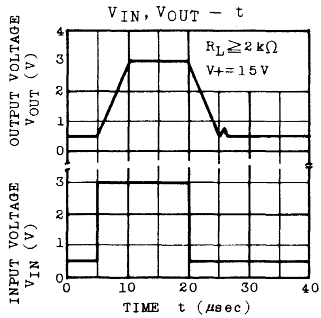


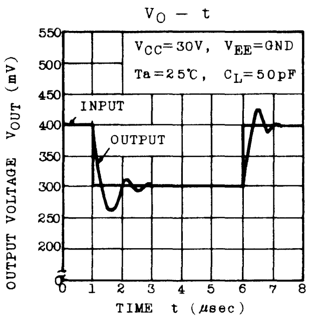


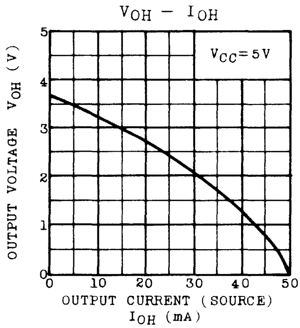


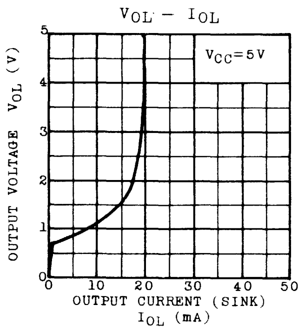
TA75358P


VOp-p — f
MAXIMUM OUTPUT VOLTAGE SWING VOp-p (Vp-p)
FREQUENCY f (Hz)
100kΩ
+15V
1kΩ
VIN
+7V
VOUT
2kΩ
20
15
10
5
0
1k
10k
100k
1M


VIN, VOUT — t
OUTPUT VOLTAGE VOUT (V)
INPUT VOLTAGE VIN (V)
RL≧2kΩ
V+=15V
TIME t (μsec)
0
10
20
30
40


VO — t
VCC=30V, VEE=GND
Ta=25℃, CL=50pF
INPUT
OUTPUT
OUTPUT VOLTAGE VOUT (mV)
TIME t (μsec)
550
500
450
400
350
300
250
200
0
1
2
3
4
5
6
7
8


VOH — IOH
VCC=5V
OUTPUT VOLTAGE VOH (V)
OUTPUT CURRENT (SOURCE)
IOH (mA)
0
10
20
30
40
50


VOL — IOL
VCC=5V
OUTPUT VOLTAGE VOL (V)
OUTPUT CURRENT (SINK)
IOL (mA)
0
10
20
30
40
50

BIPOLAR LINEAR INTEGRATED CIRCUIT
SILICON MONOLITHIC

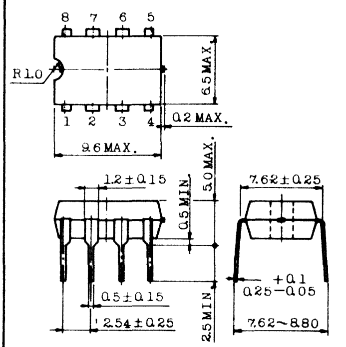
TA75393P, TA75393S

COMMUNICATION AND INDUSTRIAL USE

DUAL COMPARATOR

. Be possible to operate at the Wide Range Single or Two Supply Voltage.
. Low Supply Current : I_{CC}=0.8mA (Typ.)
. Low Input Offset Voltage : V_{IO}=2mV (Typ.)
. Wide Common Mode Input Voltage : $0 \sim V_{CC}$-1.5V_{DC}
. Output is compatible with TTL, DTL, MOS and C-MOS
. Output is Open Collector and Wired-OR possible

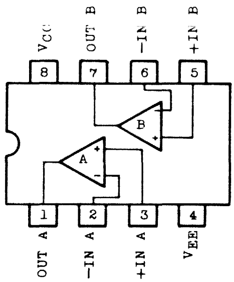
Unit in mm



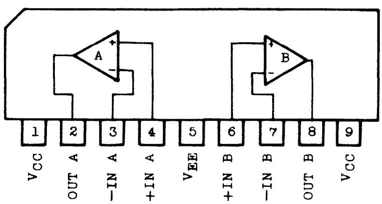
JEDEC	—
TOSHIBA	5−10C

PIN CONNECTION (TOP VIEW)

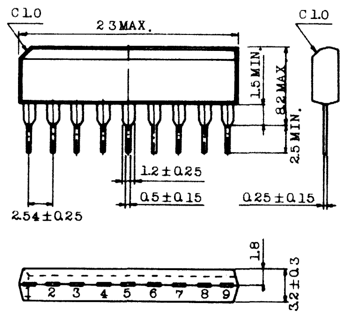
TA75393P



TA75393S



Unit in mm



Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 lead.

JEDEC	—
TOSHIBA	5−23B

TA75393P, TA75393S

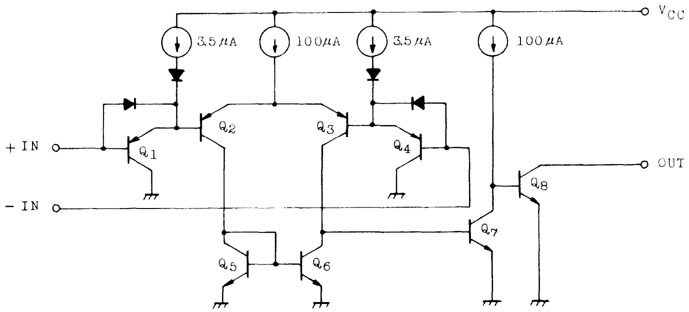
MAXIMUM RATINGS (Ta=25 °C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	±18 ~ 36	V
Differential Input Voltage	DV_{IN}	±36	V
Common Mode Input Voltage	CMV_{IN}	-0.3 ~ V_{CC}	V
Power Dissipation	P_D	500	mW
Operating Temperature	Topr	-40 ~ 85	°C
Storage Temperature	Tstg	-55 ~ 125	°C

ELECTRICAL CHARACTERISTICS (V_{CC}=5V, Ta=25°C)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	V_{IO}	4	V_O=1.4V	-	2	5	mV
Input Bias Current	I_I	2	-	-	25	250	nA
Input Offset Current	I_{IO}	2	-	-	5	50	nA
Common Mode Input Voltage	CMV_{IN}	4	-	0	-	V_{CC} -1.5	V
Voltage Gain	G_V	-	R_L=15kΩ	-	200	-	V/mV
Supply Current	I_{CC}	1	No Load	-	0.8	2	mA
Sink Current	I_{SINK}	5	+IN=0V, -IN=1V, V_{OL}=1.5V	6	16	-	mA
Output Current ("L" Level)	V_{OL}	5	+IN=0V, -IN=1V, Isink=3mA	-	0.2	0.4	V
Output Leak Current	I_{LEAK}	3	+IN=1V, -IN=0V V_O=5V	-	0.1	-	nA
Response Time	trsp	6	R_L=5.1kΩ, C_L=15pF	-	1.3	-	μs

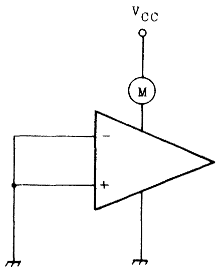
EQUIVALENT CIRCUIT



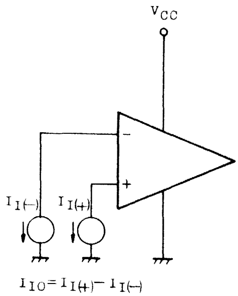
TA75393P, TA75393S

TEST CIRCUIT

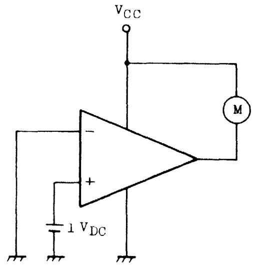
(1) I_{CC}



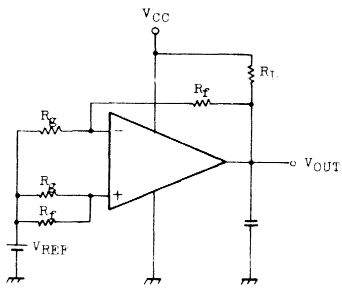
(2) I_I, I_{IO}



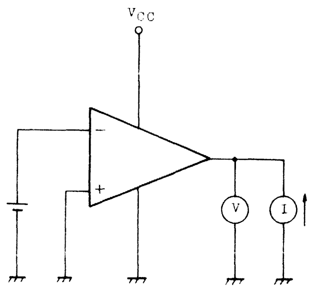
(3) I_{LEAK}



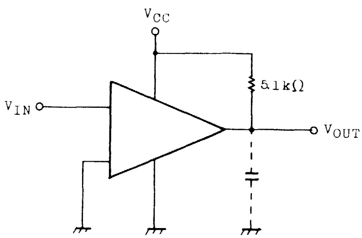
(4) V_{IO}, CMV_{IN}



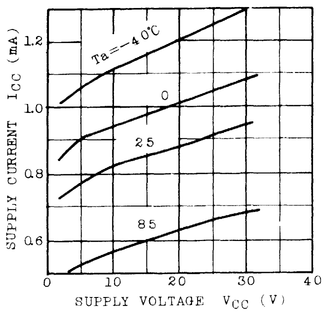
(5) I_{SINK}, V_{OL}

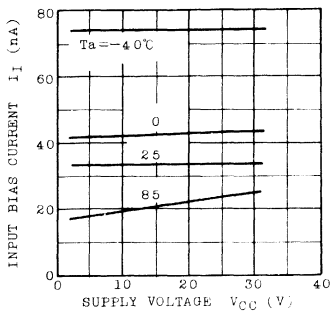


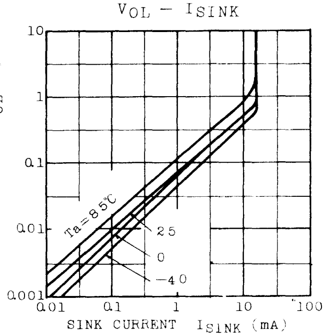
(6) t_{rsp}

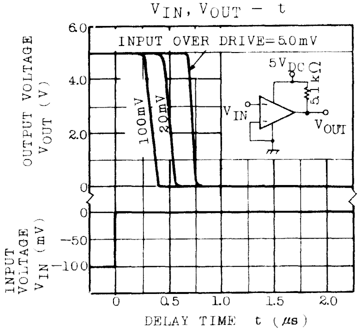


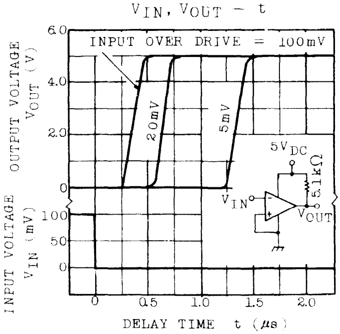
TA75393P, TA75393S











BIPOLAR LINEAR INTEGRATED CIRCUIT
SILICON MONOLITHIC

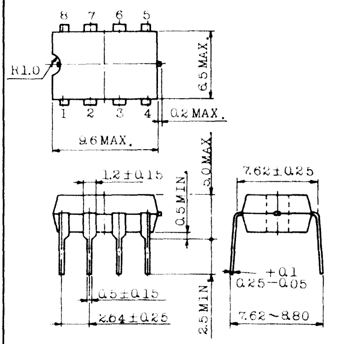
TA75458P, TA75458S

COMMUNICATION AND INDUSTRIAL USE

DUAL OPERATIONAL AMPLIFIER
OPERATIONAL AMPLIFIER
DC AMPLIFIER

- . Pair of Internally Compensated High Performance Amplifier
- . No Frequency Compensation Required
- . No Latch-up
- . Short Circuit Protection
- . Wide Common Mode and Differential Voltage Range
- . Low Power Consumption

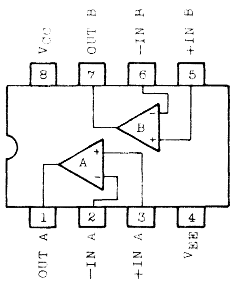
Unit in mm



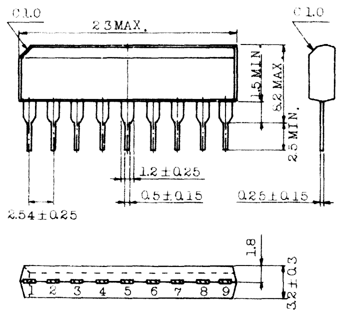
JEDEC	—
TOSHIBA	5−10C

PIN CONNECTION (TOP VIEW)

TA75458P



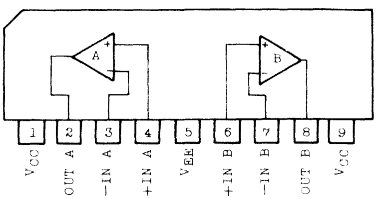
Unit in mm



Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 lead.

JEDEC	—
TOSHIBA	5−23B

TA75458S

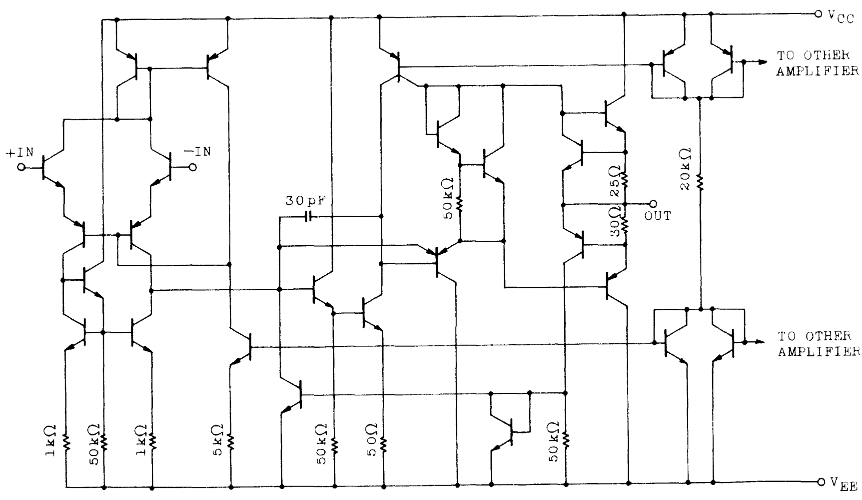


TA75458P, TA75458S

MAXIMUM RATINGS (Ta=25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Supply Voltage		V_{CC}	+18	V
		V_{EE}	-18	
Differential Input Voltage		DV_{IN}	±30	V
Input Voltage		V_{IN}	$V_{CC} \sim V_{EE}$	V
Power Dissipation	TA75458P	P_D	300	mW
	TA75458S		400	
Operating Temperature		Topr	-30 ~ 75	°C
Ambient Temperature		Tstg	-55 ~ 125	°C

EQUIVALENT CIRCUIT



TA75458P, TA75458S

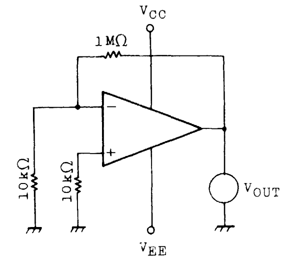
ELECTRICAL CHARACTERISTICS (V_{CC}=+15V, V_{EE}=−15V, Ta=25°C)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage		V_{IO}	1	$R_g \leq 10k\Omega$	-	1	5	mV
Input Offset Current		I_{IO}	2		-	20	200	nA
Input Bias Current		I_I	2		-	80	500	nA
Common Mode Input Voltage		CMV_{IN}	3		±12	±13	-	V
Maximum Output Voltage		V_{OM}	4	R_L=10kΩ	±12	±14	-	V
		V_{OMR}	4	R_L=2kΩ	±10	±13	-	V
Source Current		I_{source}	4		-	20	-	mA
Sink Current		I_{sink}	4		-	20	-	mA
Differential Input Impedance	Parallel Input Resistance	R_{ip}	-	f=20Hz Open Loop	0.3	1.0	-	MΩ
	Parallel Input Capacitance	C_{ip}	-	f=20Hz Open Loop	-	6.0	-	pF
Output Impedance		Z_O	-	f=20Hz	-	75	-	Ω
Voltage Gain (Open Loop)		G_V	7	V_{OUT}=±10V, R_L=2kΩ	86	100	-	dB
Common Mode Input Signal Rejection Ratio		CMRR	3	f=100Hz	70	90	-	dB
Supply Voltage Rejection Ratio		SVRR	1	$R_g \leq 10k\Omega$	-	30	150	μV/V
Power Bandwidth		f_W	-	G_V=1, R_L=2kΩ V_{OUT}=20V_{p-p}	-	14	-	kHz
Slew Rate		SR	6	G_V=1, R_L=2kΩ	-	0.8	-	V/μs
Unity Gain Cross Frequency		f_T	7	Open Loop	-	1.1	-	MHz
Power Dissipation		P_D	5	V_O=0	-	70	170	mW
Input Offset Voltage Drift		$\Delta V_{IO}/\Delta T$	1	$R_g \leq 10k\Omega$ Ta=−30 ~75°C	-	-	50	μV/°C
Supply Current		I_{CC}, I_{EE}	5		-	2.3	5.6	mA

TA75458P, TA75458S

TEST CIRCUIT

(1) V_{IO}, $\Delta V_{IO}/\Delta T$, SVRR



$V_{IO}=V_{OUT}/100$ (V)

$\Delta V_{IO}/\Delta T=\{V_{IO}(25°C)-V_{IO}(-30°C)\}/55$ (V/°C)

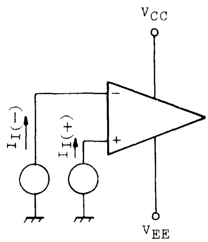
$\Delta V_{IO}/\Delta T=\{V_{IO}(75°C)-V_{IO}(25°C)\}/50$ (V/°C)

$SVRR=(V_{IO1}-V_{IO2})/5$ (μV/V)

V_{IO1} : V_{CC}, AT $V_{EE}=\pm 17.5V$

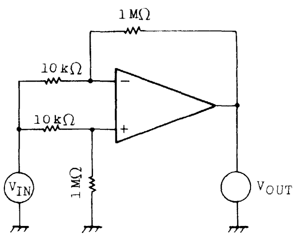
V_{IO2} : V_{CC}, AT $V_{EE}=\pm 12.5V$

(2) I_I, I_{IO}



$|I_{IO}=I_I(+)-I_I(-)|$

(3) CMV_{IN}, CMRR



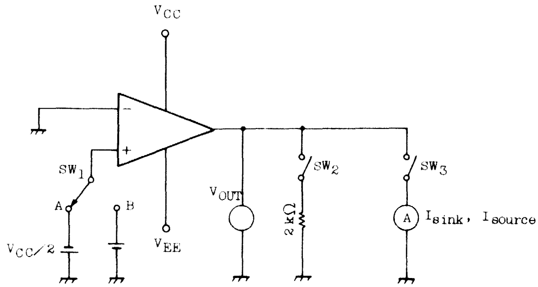
CMV_{IN} : $V_{OUT}=\pm 1V$ (DC)

V_{IN}=MEASURE

CMRR : RATIO OF G_{diff} vs G_{CM}

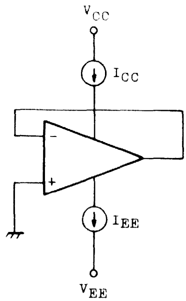
$CMRR=20\ \ell og\ \frac{G_{diff}}{G_{CM}}$ (dB)

(4) V_{OM}, V_{OMR}, I_{sink}, I_{source}



$V_{OM(+)}$	:	SW_1 IS SIDE B,	SW_2 IS OPEN,	SW_3 IS OPEN
$V_{OM(-)}$	:	SW_1 IS SIDE A,	SW_2 IS OPEN,	SW_3 IS OPEN
$V_{OMR(+)}$	:	SW_1 IS SIDE B,	SW_2 IS CLOSE,	SW_3 IS OPEN
$V_{OMR(-)}$	:	SW_1 IS SIDE A,	SW_2 IS CLOSE,	SW_3 IS OPEN
I_{sink}	:	SW_1 IS SIDE A,	SW_2 IS OPEN,	SW_3 IS CLOSE
I_{source}	:	SW_1 IS SIDE B,	SW_2 IS OPEN,	SW_3 IS CLOSE

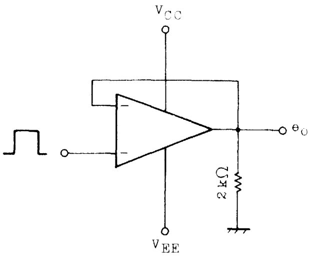
(5) I_{CC}, I_{EE}, P_D

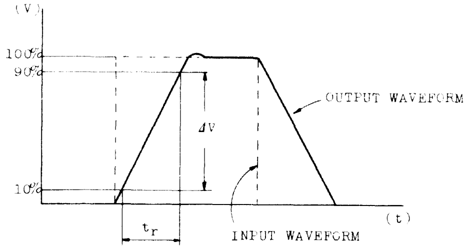


$P_D = V_{CC} \cdot I_{CC} + V_{EE} \cdot I_{EE}$ (W)

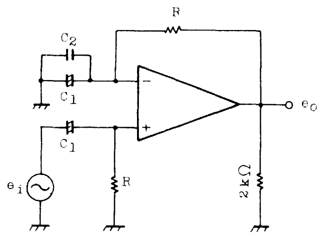
TA75458P, TA75458S

(6) SR





(7) G_V, f_T



G_V

$R \gg 1/WC_1$

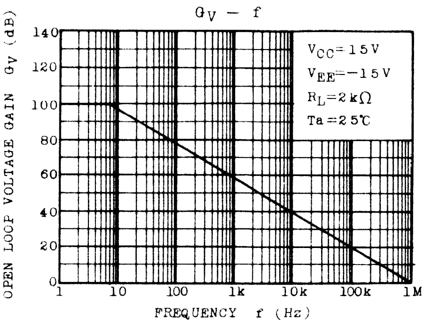
C_1 : COUPLING CONDENSER

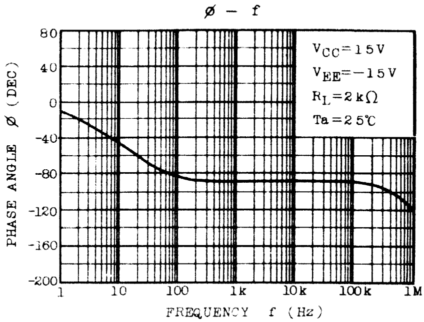
C_2 : HIGH FREQUENCY BYPASS CONDENSER

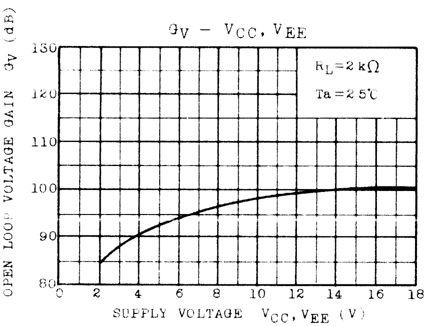
$0.1\mu F$

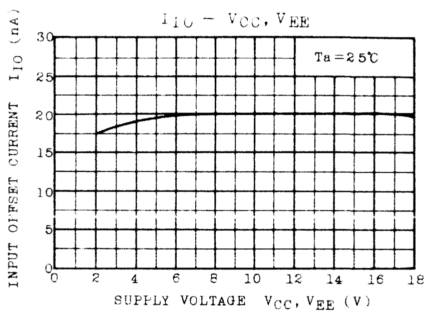
$G_V = 20 \log e_o/e_i$ (dB)

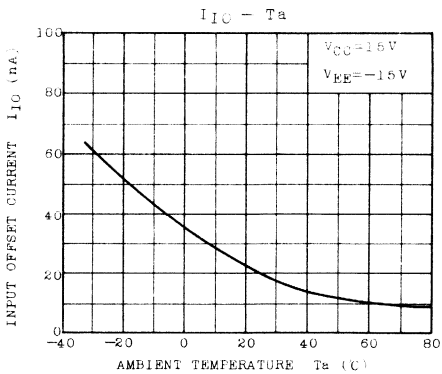
f_T INPUT FREQUENCY AT $e_i = e_o$

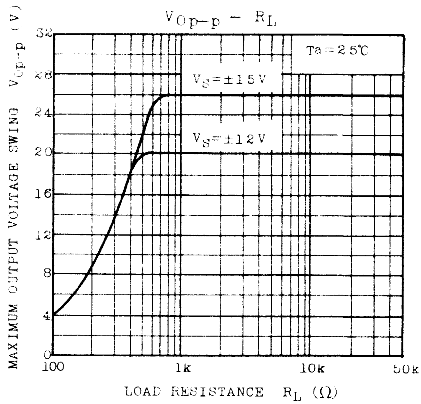

G_V — f
V_{CC}=15V
V_{EE}=−15V
R_L=2kΩ
Ta=25℃
OPEN LOOP VOLTAGE GAIN G_V (dB)
FREQUENCY f (Hz)


ø — f
V_{CC}=15V
V_{EE}=−15V
R_L=2kΩ
Ta=25℃
PHASE ANGLE ø (DEC)
FREQUENCY f (Hz)

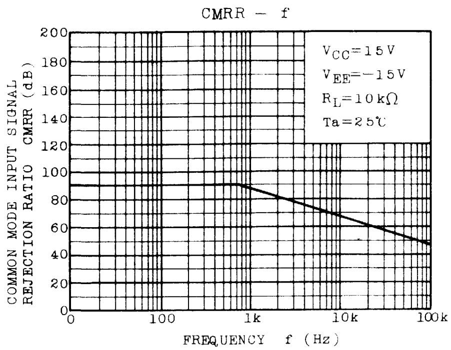

G_V — V_{CC}, V_{EE}
R_L=2kΩ
Ta=25℃
OPEN LOOP VOLTAGE GAIN G_V (dB)
SUPPLY VOLTAGE V_{CC}, V_{EE} (V)

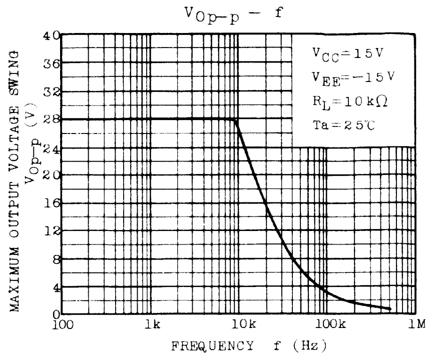

I_{IO} — V_{CC}, V_{EE}
Ta=25℃
INPUT OFFSET CURRENT I_{IO} (nA)
SUPPLY VOLTAGE V_{CC}, V_{EE} (V)

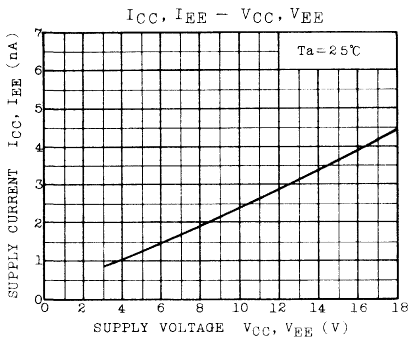

I_{IO} — Ta
V_{CC}=15V
V_{EE}=−15V
INPUT OFFSET CURRENT I_{IO} (nA)
AMBIENT TEMPERATURE Ta (℃)


V_{Op-p} — R_L
Ta=25℃
V_S=±15V
V_S=±12V
MAXIMUM OUTPUT VOLTAGE SWING V_{Op-p} (V)
LOAD RESISTANCE R_L (Ω)

TA75458P, TA75458S







BIPOLAR LINEAR INTEGRATED CIRCUIT
SILICON MONOLITHIC

TA75557P, TA75557S

COMMUNICATION AND INDUSTRIAL USE

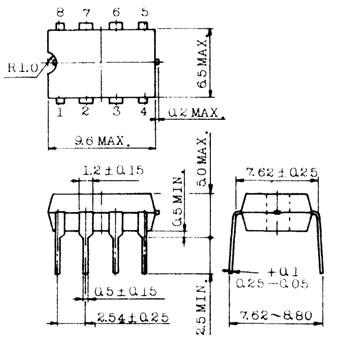
DUAL LOW NOISE OPERATIONAL AMPLIFIER

Internal Frequency Compensation Type

Pin Compatible with TA75458P and TA75458S

- Possible to exchange the position of 9 Pin for 1 Pin because of Pin Connection being symmetric (TA75557S Device Only)
- Wide Band Range : f=3MHz (Typ.)
- Suitable application for Active Filter, Equalizer Amp. and Headphone Amp.

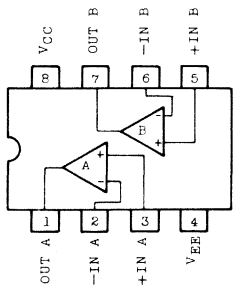
Unit in mm



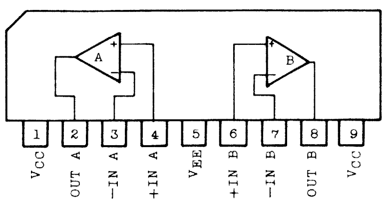
JEDEC	−
TOSHIBA	5−10C

PIN CONNECTION (TOP VIEW)

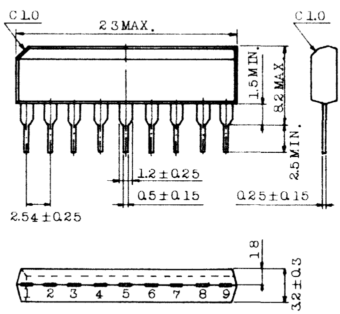
TA75557P



TA75557S



Unit in mm



Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 lead.

JEDEC	−
TOSHIBA	5−23B

TA75557P, TA75557S

MAXIMUM RATINGS (Ta=25°C)

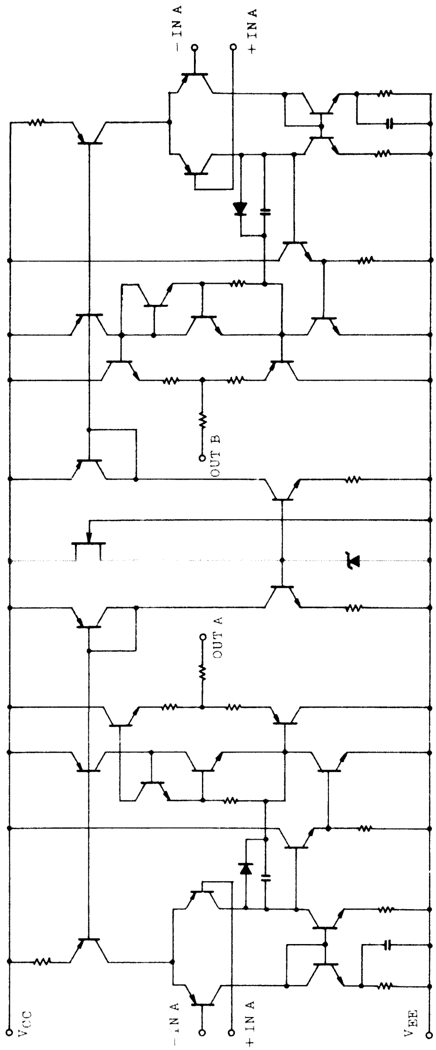
CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC} V_{EE}	+18 -18	V
Differential Input Voltage	DV_{IN}	±30	V
Input Voltage	V_{IN}	$V_{CC} \sim V_{EE}$	V
Power Dissipation	P_D	500	mW
Operating Temperature	T_{opr}	-40 ~ 85	°C
Storage Temperature	T_{stg}	-55 ~ 125	°C

ELECTRICAL CHARACTERISTICS (V_{CC}=15V, V_{EE}=-15V, Ta=25°C)

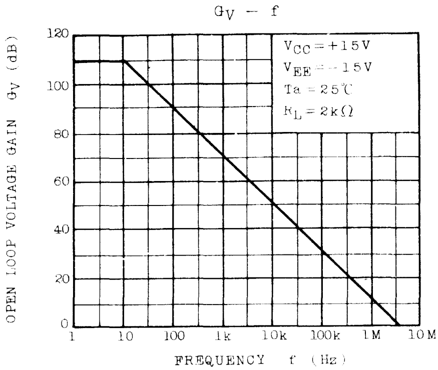
CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	V_{IO}	-	$R_G \leqq 10k\Omega$	-	0.5	6	mV
Input Offset Current	I_{IO}	-	-	-	5	200	nA
Input Bias Current	I_I	-	-	-	60	500	nA
Common Mode Input Voltage	CMV_{IN}	-	-	±12	±14	-	V
Maximum Output Voltage	V_{OM}	-	R_L=10kΩ	±12	±14	-	V
	V_{OMR}		R_L=2kΩ	±10	±13	-	
Source Current	I_{source}	-	-	27	-	-	mA
Sink Current	I_{sink}	-	-	27	-	-	mA
Voltage Gain (Open Loop)	G_V	-	V_{OUT}=±10V, R_L=2kΩ	86	100	-	dB
Common Mode Input Signal Rejection Ratio	CMRR	-	$R_g \leqq 10k\Omega$	70	90	-	dB
Supply Voltage Rejection Ratio	SVRR	-	$R_g \leqq 10k\Omega$	-	30	150	μV/V
Slew Rate	SR	-	G_V=1, R_L=2kΩ	-	1.0	-	V/μs
Unity Gain Cross Frequency	f_T	-	Open Loop	-	3.0	-	MHz
Supply Current	I_{CC}, I_{EE}	-	-	-	4.0	6.0	mA
Equivalent Input Noise Voltage	V_{NI}	-	R_S=1kΩ, f=30Hz~30kHz	-	2.5	-	μV_{rms}

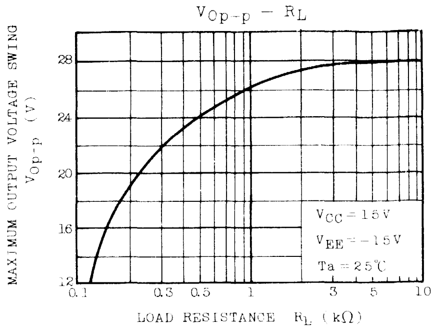
TA75557P, TA75557S

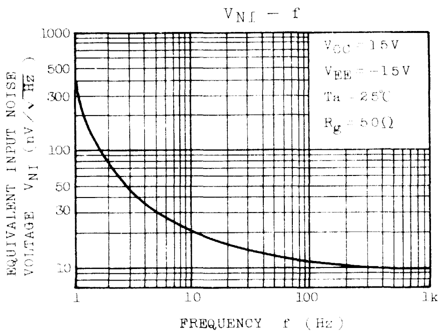
EQUIVALENT CIRCUIT

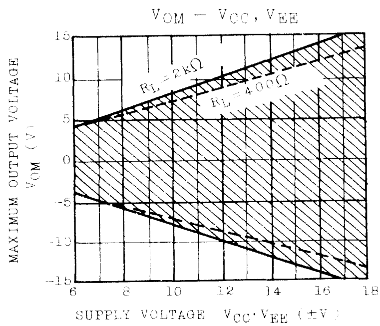


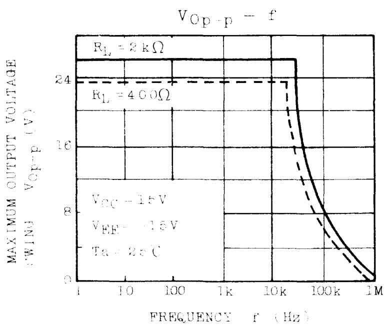
TA75557P, TA75557S

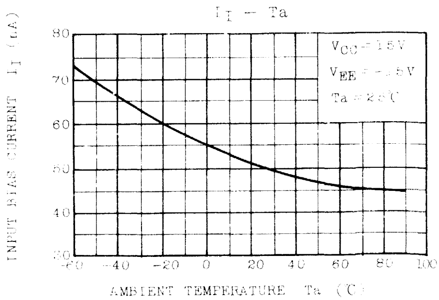












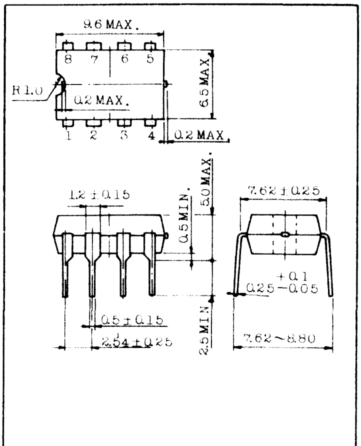
BIPOLAR LINEAR INTEGRATED CIRCUIT
SILICON MONOLITHIC

TA75558P, TA75558S

DUAL LOW NOISE OPERATIONAL AMPLIFIER

- Internal Frequency Compensation Type.
- Pin Compatible with TA75458P and TA75458S
- Possible to Exchange the Position of 9 Pin for 1 Pin Because of Pin Connection Being Symmetric. (TA75558S Device Only)
- Wide Band Range : f_T=3MHz (Typ.)
- Suitable Application for Active Filter Equalizer Amplifier and Headphone Amplifier.

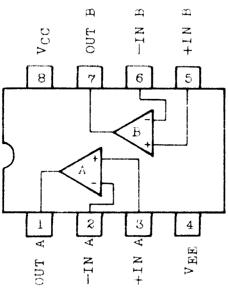
Unit in mm



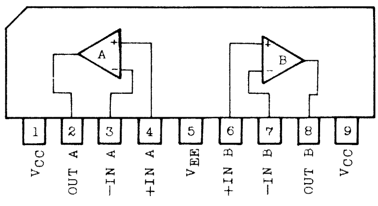
JEDEC	—
TOSHIBA	5−10C

PIN CONNECTION (TOP VIEW)

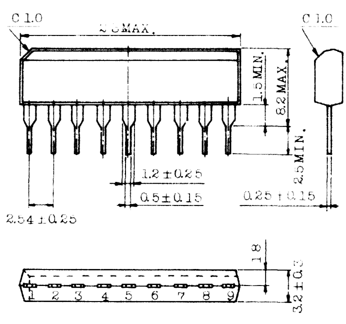
TA75558P



TA75558S



Unit in mm



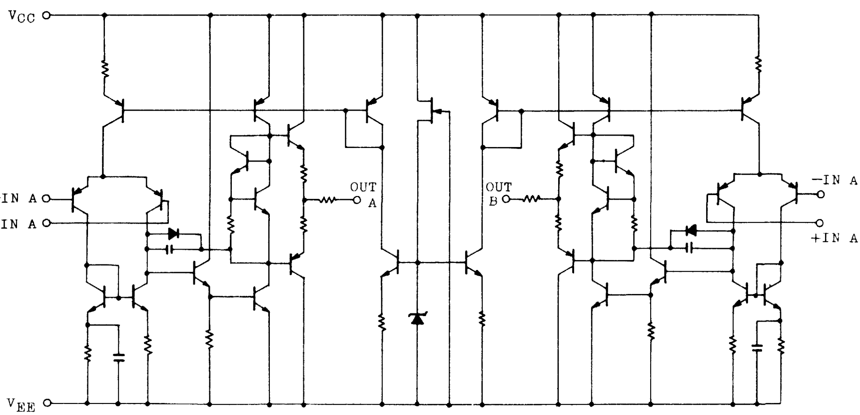
JEDEC	—
TOSHIBA	5−23B

TA75558P, TA75558S

MAXIMUM RATINGS (Ta=25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}, V_{EE}	+18, -18	V
Differential Voltage	DV_{IN}	±30	V
Input Voltage	V_{IN}	$V_{CC}\sim V_{EE}$	V
Power Dissipation	P_D	500	mW
Operating Temperature	Topr	-40 ~ 85	°C
Storage Temperature	Tstg	-55 ~ 125	°C

EQUIVALENT CIRCUIT

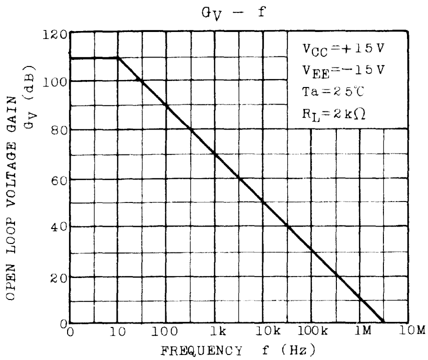


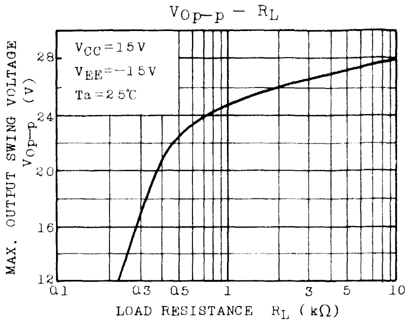
TA75558P, TA75558S

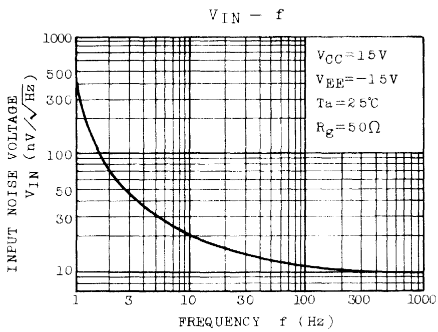
ELECTRICAL CHARACTERISTICS (V_{CC}=15V, V_{EE}=-15V, Ta=25°C)

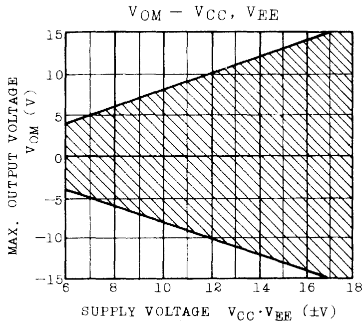
CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	V_{IO}	$R_g \leqq 10k\Omega$	-	0.5	6	mV
Input Offset Voltage	I_{IO}		-	5	200	nA
Input Biase Current	I_I		-	60	500	nA
Common Mode Input Voltage	CMV_{IN}		±12	±14	-	V
Maximum Output Voltage	V_{OM}	R_L=10kΩ	±12	±14	-	V
	V_{OMR}	R_L=2kΩ	±10	±13	-	
Source Current	I_{source}		-	40	-	mA
Sink Current	I_{sink}		-	40	-	mA
Voltage Gain (Open Loop)	GV	V_{OUT}=±10V, R_L=2kΩ	86	100	-	dB
Common Mode Rejection Ratio	CMRR	$R_g \leqq 10k\Omega$	70	90	-	dB
Supply Voltage Rejection Ratio	SVRR	$R_g \leqq 10k\Omega$	-	30	150	μV/V
Slew Rate	SR	Gv=1, R_L=3kΩ		1.0	-	V/μs
Unity Gain Cross Frequency	f_T	Open Loop	-	3.0	-	MHz
Supply Current	I_{CC}, I_{EE}		-	4.0	6.0	mA
Input Noise Voltage	V_N	R_S=1kΩ , f=30Hz ~30kHz	-	2.5	-	μVrms

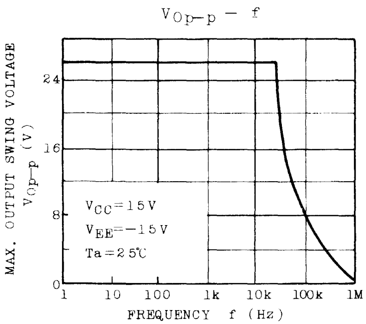
TA75558P, TA75558S

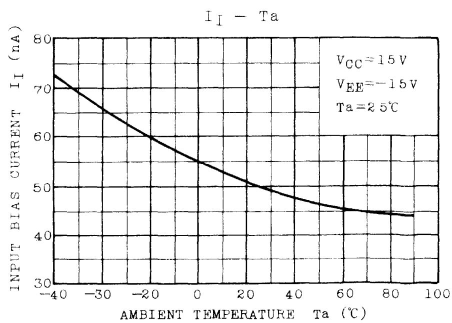












BIPOLAR LINEAR INTEGRATED CIRCUIT
SILICON MONOLITHIC

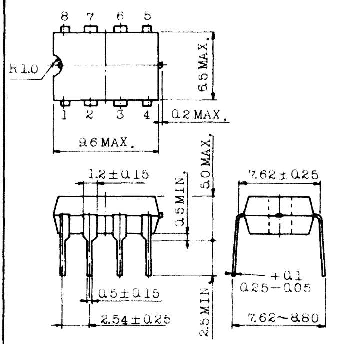
TA75559P, TA75559S

COMMUNICATION AND INDUSTRIAL USE

DUAL LOW NOISE OPERATIONAL AMPLIFIER

- Internal Frequency Compensation Type
- Pin Compatible with TA75458P and TA75458S
- Possible to exchange the position of 9 Pin for 1 Pin because of Pin connection being Symmetric. (TA75559S Device Only)
- Wide Band Range : f_T=5MHz (Typ.)
- Suitable Ampplication for Active Filter, Equalizer Amp, and Headphone Amp.

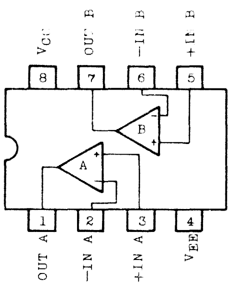
Unit in mm



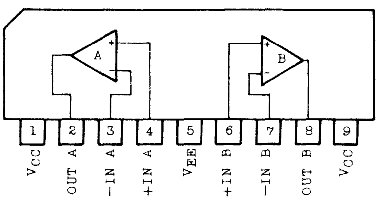
JEDEC	–
TOSHIBA	5–10C

PIN CONNECTION (TOP VIEW)

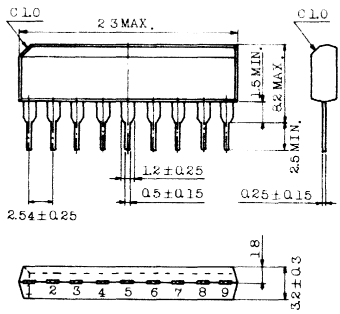
TA75559P



TA75559S



Unit in mm



Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 lead.

JEDEC	–
TOSHIBA	5–23B

TA75559P, TA75559S

MAXIMUM RATINGS (Ta=25°C)

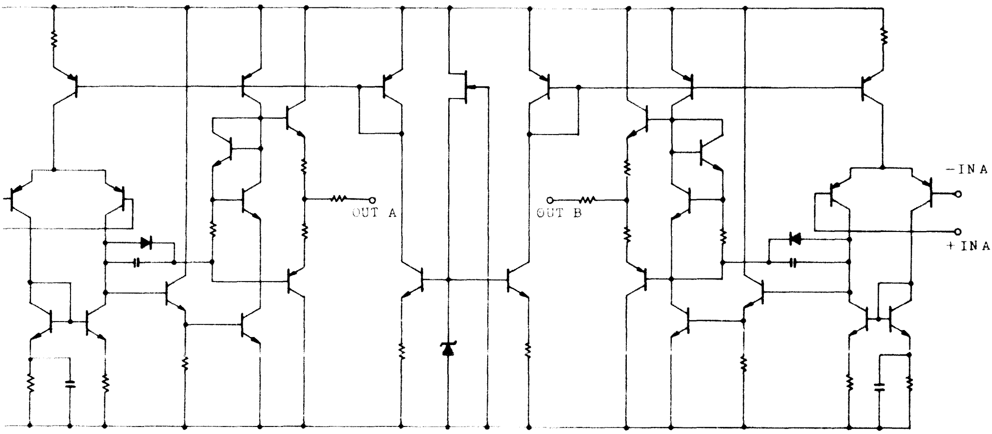
CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	+18	V
	V_{EE}	-18	
Differential Input Voltage	DV_{IN}	±30	V
Input Voltage	V_{IN}	$V_{CC} \sim V_{EE}$	V
Power Dissipation	P_D	500	mW
Operating Temperature	Topr	-40 ~ 85	°C
Storage Temperature	Tstg	-55 ~ 125	°C

ELECTRICAL CHARACTERISTICS (V_{CC}=15V, V_{EE}=-15V, Ta=25°C)

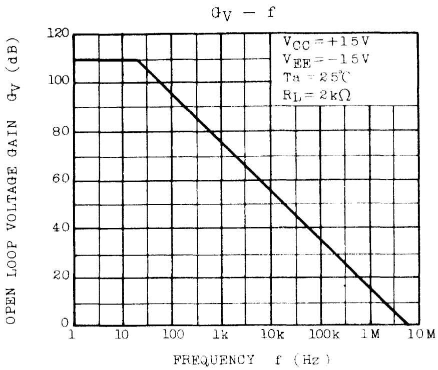
CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	V_{IO}	-	$R_g \leq 10k\Omega$	-	0.5	6	mV
Input Offset Current	I_{IO}	-	-	-	5	200	nA
Input Bias Current	I_I	-	-	-	60	500	nA
Common Mode Input Voltage	CMV_{IN}	-	-	±12	±14	-	V
Maximum Output Voltage	V_{OM}	-	$R_L=10k\Omega$	±12	±14	-	V
	V_{OMR}		$R_L=2k\Omega$	±10	±13	-	
Source Current	I_{source}	-	-	-	40	-	mA
Sink Current	I_{sink}	-	-	-	40	-	mA
Voltage Gain (Open Loop)	G_V	-	$V_{OUT}=\pm10V$, $R_L=2k\Omega$	86	100	-	dB
Common Mode Input Signal Rejection Ratio	CMRR	-	$R_g \leq 10k\Omega$	70	90	-	dB
Supply Voltage Rejection Ratio	SVRR	-	$R_g \leq 10k\Omega$	-	30	150	μV/V
Slew Rate	SR	-	$G_V=1$, $R_L=2k\Omega$	-	2.0	-	V/μs
Unity Gain Cross Frequency	f_T	-	Open Loop	-	5.0	-	MHz
Supply Current	I_{CC}, I_{EE}	-	-	-	4.0	6.0	mA
Equivalent Input Noise Voltage	V_{NI}	-	$R_S=1k\Omega$, f=30Hz~30kHz	-	2.5	-	μV_{rms}

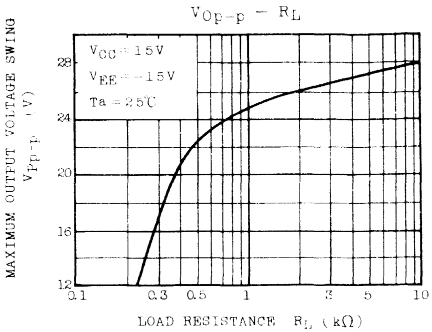
TA75559P, TA75559S

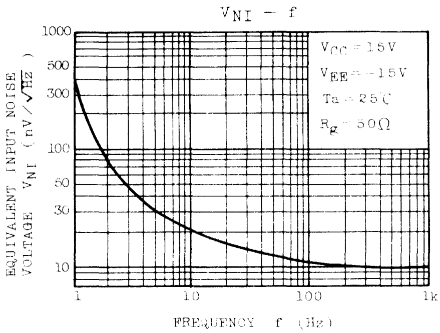
EQUIVALENT CIRCUIT

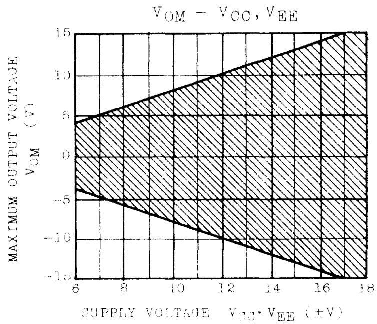


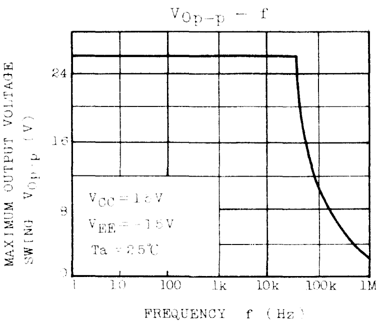
TA75559P, TA75559S

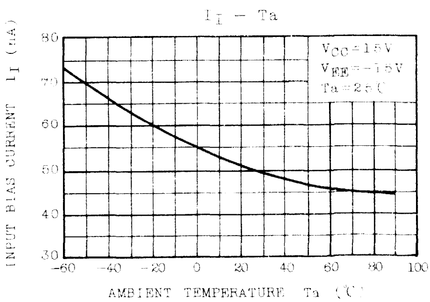












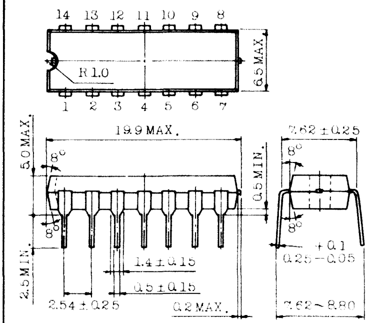
BIPOLAR LINEAR INTEGRATED CIRCUIT
SILICON MONOLITHIC

TA75902P

OPERATIONAL AMPLIFIER
DC AMPLIFIER

. In the linear mode the input Common Mode Voltage Range includes ground.
. Four Internally Compensated OP Amp is single package.
. Low power dissipation and power drain suitable for battery operation.
. Differential Input Voltage Range equal to the Power Supply Voltage.
. Wide Power Supply Voltage Range and Signal Power Supply: Single Supply $3V_{DC}$ to $36V_{DC}$
Dual Supplies $\pm 1.5V_{DC}$ to $\pm 18V_{DC}$
. Large Output Voltage Swing: $0V_{DC}$ to $V_{CC}-1.5V_{DC}$
. Low Input Biasing Current: $I_I=45nA_{DC}$ (Typ.)

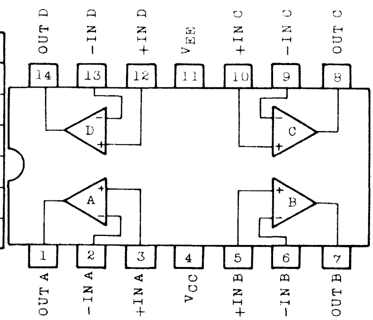
Unit in mm



Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.14 leads.

JEDEC	—
TOSHIBA	5−21F

PIN CONNECTION (TOP VIEW)



MAXIMUM RATINGS (Ta=25°C)

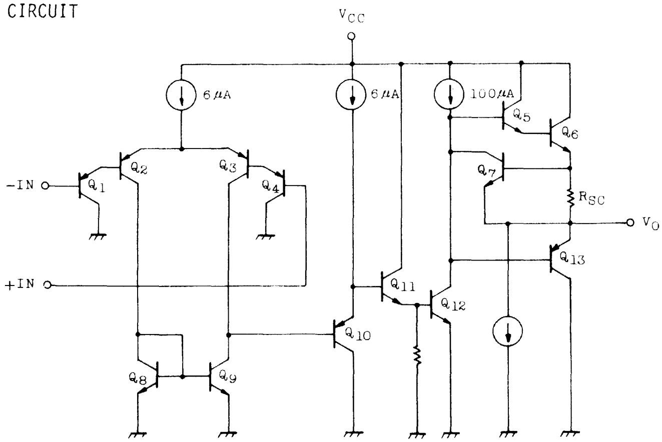
CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}, V_{EE}	±18, 36	V
Differential Input Voltage	DV_{IN}	±36	V
Input Voltage	V_{IN}	-0.3 ~ 36	V
Power Dissipation	P_D	625	mW
Operating Temperature	Topr	-40 ~ 85	°C
Storage Temperature	Tstg	-55 ~ 125	°C

TA75902P

ELECTRICAL CHARACTERISTICS (V_{CC}=5V, V_{EE}=GND, Ta=25°C)

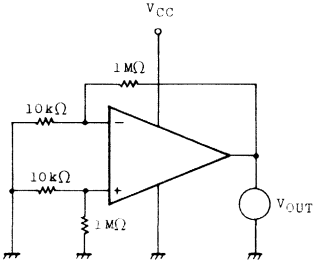
CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	V_{IO}	1	$R_g \leqq 10k\Omega$	–	2	7	mV
Input Offset Current	I_{IO}	2	–	–	5	30	nA
Input Bias Current	I_I	2	–	–	45	150	nA
Common Mode Input Voltage	CMV_{IN}	3	V_{CC}=30V, V_{EE}=GND	0	–	V_{CC} -1.5	V
Supply Current	I_{CC}, I_{EE}	4	$R_L=\infty$, All OP Amps	–	0.7	1.2	mA
Voltage Gain	G_V	5	$R_L \geqq 2k\Omega$	86	100	–	dB
Maximum Output Voltage Swing	V_{Op-p}	6	$R_L=2k\Omega$	0	–	V_{CC} -1.5	V
Common Mode Input Signal Rejection Ratio	CMRR	3	–	60	85	–	dB
Supply Voltage Rejection Ratio	SVRR	1	$R_g=10k\Omega$	60	100	–	dB
Source Current	I_{source}	6	$-IN=0V_{DC}$, $+IN=1V_{DC}$	20	40	–	mA
Sink Current	I_{sink}	6	$-IN=1V_{DC}$, $+IN=0V_{DC}$	10	20	–	mA

EQUIVALENT CIRCUIT



TEST CIRCUIT

(1) V_{IO}, SVRR



. $V_{IO}=V_{OUT}/100$

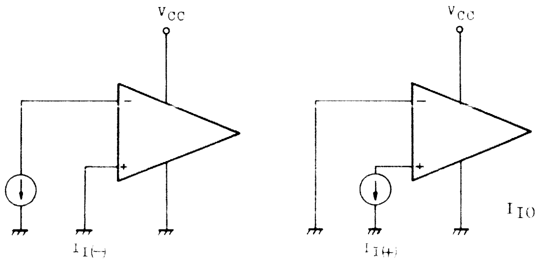
. SVRR=20 logE(dB)

$$E = \left| \frac{V_{OUT1}-V_{OUT2}}{V_{CC1}-V_{CC2}} \right| \times \frac{1}{100}$$

V_{OUT1} : V_{OUT} (V_{CC1}=5V)

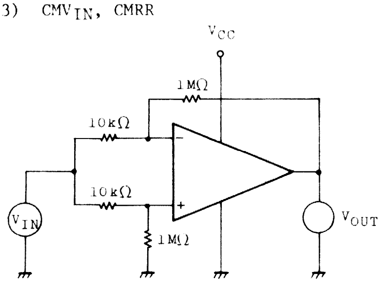
V_{OUT2} : V_{OUT} (V_{CC2}=10V)

(2) I_I, I_{IO}



$I_{IO} = \left| I_{I(-)} - I_{I(+)} \right|$

(3) CMV_{IN}, CMRR



. CMRR=20 log G_D/G_C (dB)

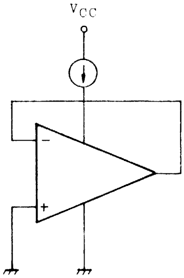
G_D : DIFFERENTIAL VOLTAGE GAIN

G_C : COMMON MODE VOLTAGE GAIN

. CMV_{IN} : V_{IN}=0V, V_{CC}-1.5V SUPPLES

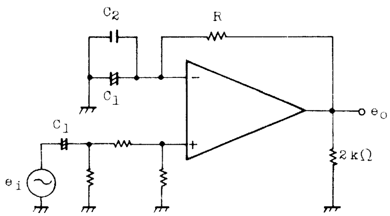
TA75902P

(4) I_{CC}



. I_{CC} : (V_{CC}=5V)

(5) G_V

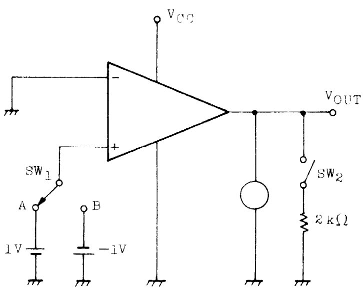


. G_V=20 log e_o/e_i(dB)
$R \gg 1/WC_1$

. C_1 : CUPLING CONDENSER

. C_2 : HIGH FREQUENCY BYPASS CONDENSER

(6) V_{Op-p}, I_{source}, I_{sink}

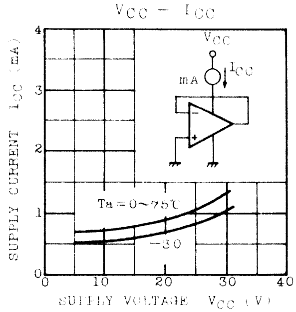


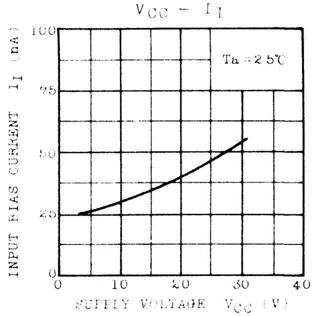
. V_{Op-p};
V_{OH} : SW_1 IS SIDE A
V_{OL} : SW_1 IS SIDE B

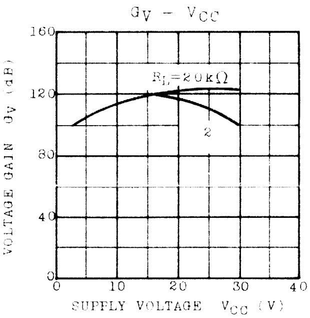
. I_{source}
SW_1 IS SIDE A
V_{OUT} → 0V MEASURE

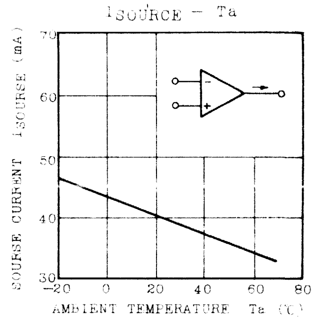
. I_{sink}
SW_1 IS SIDE B
V_{OUT} → 5V MEASURE

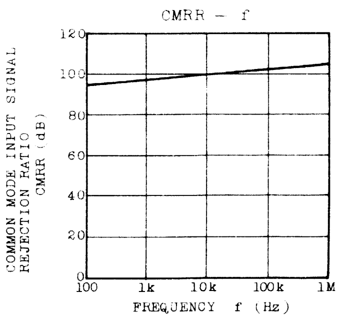
TA75902P

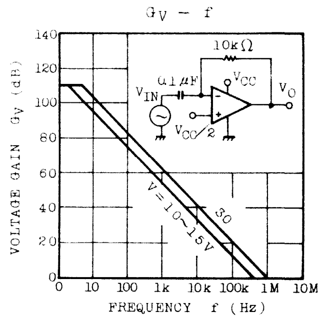

VCC − ICC
VCC
mA
ICC
Ta = 0~75℃
−30
SUPPLY CURRENT ICC (mA)
SUPPLY VOLTAGE VCC (V)
0
10
20
30
40
1
2
3
4


VCC − II
Ta = 25℃
INPUT BIAS CURRENT II (nA)
SUPPLY VOLTAGE VCC (V)
0
10
20
30
40
25
50
75
100

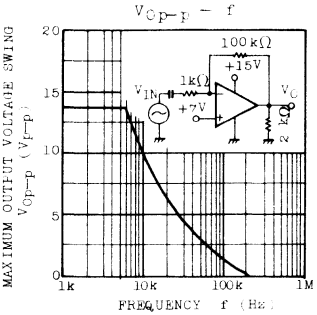

GV − VCC
RL = 20kΩ
2
VOLTAGE GAIN GV (dB)
SUPPLY VOLTAGE VCC (V)
0
10
20
30
40
40
80
120
160

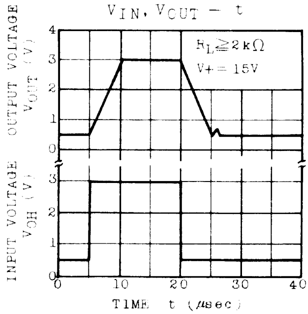

ISOURCE − Ta
SOURSE CURRENT ISOURSE (mA)
AMBIENT TEMPERATURE Ta (℃)
−20
0
20
40
60
80
30
40
50
60
70

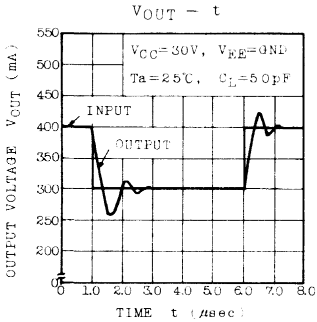

CMRR − f
COMMON MODE INPUT SIGNAL REJECTION RATIO CMRR (dB)
FREQUENCY f (Hz)
100
1k
10k
100k
1M
0
20
40
60
80
100
120

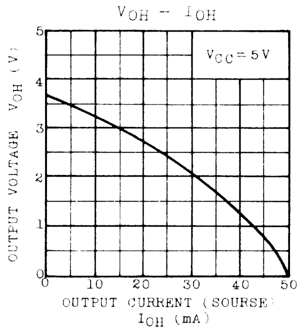

GV − f
10kΩ
0.1μF
VCC
VIN
VO
VCC/2
V = 10~15V
30
VOLTAGE GAIN GV (dB)
FREQUENCY f (Hz)
0
10
100
1k
10k
100k
1M
10M
20
40
60
80
100
120
140

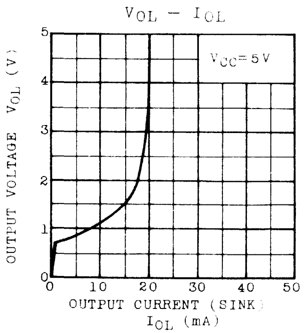
TA75902P


VOp-p − f
MAXIMUM OUTPUT VOLTAGE SWING VOp-p (Vp-p)
FREQUENCY f (Hz)
100kΩ
+15V
1kΩ
VIN
+7V
VO
2kΩ
20
15
10
5
0
1k
10k
100k
1M


VIN, VOUT − t
OUTPUT VOLTAGE VOUT (V)
INPUT VOLTAGE VOH (V)
RL≧2kΩ
V+ = 15V
TIME t (μsec)
0
10
20
30
40


VOUT − t
VCC=30V, VEE=GND
Ta=25℃, CL=50pF
INPUT
OUTPUT
OUTPUT VOLTAGE VOUT (mA)
TIME t (μsec)
550
500
450
400
350
300
250
200
0
1.0
2.0
3.0
4.0
5.0
6.0
7.0
8.0


VOH − IOH
VCC=5V
OUTPUT VOLTAGE VOH (V)
OUTPUT CURRENT (SOURSE)
IOH (mA)
0
10
20
30
40
50


VOL − IOL
VCC=5V
OUTPUT VOLTAGE VOL (V)
OUTPUT CURRENT (SINK)
IOL (mA)
0
10
20
30
40
50

CROSS REFERENCE

CROSS REFERENCE

OPERATIONAL AMPLIFIER

TOSHIBA	NS	MOT	TI	F/C	NEC	JRC
TA7502P	LM709N	MC1709P1	μA709CP	μA709TC	μPC55A	
TA7504P	LM741CN	MC1741CP1	μA741CP	μA741TC	μPC151C μPC741C	
TA7504S						
TA7506P	LM301AN	LM301AN	μA301AT	μA301AT	μPC157C μPC301AC	
TA7540P						
TA75254P					μPC254	
TA75358P	LM358N LM2904	LM358 LM2904	LM358 LM2904		μPC358C μPC1251C	NJM2904D
TA75358F		LM358D LM2904D			μPC358G μPC1251G	NJM2904M
TA75458P	LM1458N	MC1458CP1	MC1458P	μA1458TC	μPC251C μPC1458C	
TA75458S						
TA75458F		MC1458D			μPC251G μPC1458G	
TA75557P					μPC4557C	
TA75557S						
TA75557F						
TA75558P		MC4558CP1	TL4558P	μA4558TC	μPC4558C	NJM4558D
TA75558S						NJM4558S
TA75558F					μPC4558G	NJM4558M
TA75559P					μPC4559C	NJM4559D
TA75559S						NJM4559S
TA75559F						NJM4559F
TA75902P	LM2902N LM324N	LM2902N LM324N	LM2902N LM324N	μA2902 μA324	μPC451C μPC324C	NJM2902N
TA75902F		LM2902D LM324D			μPC451G μPC324G	NJM2902M

COMPARATOR & SPECIAL FUNCTION

TOSHIBA	NS	MOT	TI	F/C	NEC	JRC
TA7521P						
TA7523S						
TA7523AS						
TA75339P	LM339N LM2901N	LM339 LM2901N	LM339N	μA3302	μPC339C μPC177C	NJM2901N
TA75339F		LM339D LM2901D			μPC339G μPC177G	NJM2901M
TA75339AP						
TA75393P	LM393N LM2903N	LM393 LM2903	LM393JG		μPC393C μPC277C	NJM2903N
TA75393S						NJM2903S
TA75393F		LM393D LM2903D			μPC393G μPC277G	NJM2903M
TA75393AP						NJM2403D
TA75393AS						NJM2403M
TA7555P	LM555CN	MC1455P1	NE555P	μA555TC	μPC1555C μPC617C	NJM555D
TA7555F		MC1455D				NJM555M

Regulator

Series

ALPHANUMERIC INDEX

Regulator

TYPE NUMBERS **PAGE**

TA7089P 249
TA7179P 269
TA78005AP~TA78024AP 281
TA78M05P~TA78M24P 299
TA78L005P/AP~TA78L024P/AP 312
TA79005P~TA79024P 331

SELECTION GUIDE &
CROSS REFERENCE

Regulator IC Line Up/Selection Guide

Regulator		Type No.	Characteristics		Outline
Three Terminal Regulator	Positive	TA78***AP	1 A	5, 6, 8, 9, 10, 12 15, 18, 20, 24V	TO-220AB
		TA78M***P☆	0.5 A		TO-220AB
		TA78L***P TA78L***AP	0.15A		TO-92MOD
	Negative	TA79***P ☆	1 A	−5, −6, −8, −9, −10, −12 −15, −18, −20, −24V	TO-220AB
		TA79L***P ☆	0.15A		TO-92MOD
Tracking Regulator		TA7179P	V_{OUT} = ±15V I_{OUT} = ±0.1A		DIP-14
Variable Regulator		TA7089P	V_{OUT} = 3.3~33V I_{OUT} = 0.2A		DIP-14

☆ New Product or Under Development

Regulator IC Cross Reference

		Toshiba	F/C	TI	MOT	NS
Positive Regulator	1 A	TA78***AP	μA78**C	μA78**	MC78**	LM78**
	0.5 A	TA78M***P	μA78M**	μA78M**	MC78M**	LM78M**
	0.15A	TA78L***P TA78L***AP	μA78L**	μA78L**	MC78L**	LM78L**
Negative Regulator	1 A	TA79***P	μA79**	μA79**	MC79**	LM79**
	0.15A	TA79L***P			MC79L**	LM79L**
Tracking Regulator	±15V ±0.1A	TA7179P			MC1468L	(LM325N)
Variable Regulator	3.3~33V 0.2 A	TA7089P	μA723C			

( ): Similar Replacement

TECHNICAL DATA SHEET

BIPOLAR LINEAR INTEGRATED CIRCUIT
SILICON MONOLITHIC

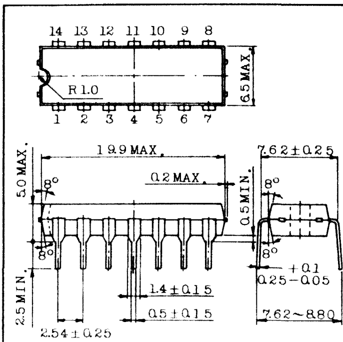
TA7089P

GENERAL PURPOSE VOLTAGE REGULATOR.

COMMUNICATION AND INDUSTRIAL USE

- Low Output Impedance : $Z_O = 40m\Omega$ (Typ.)
- High Ripple Rejection : RR=48dB(Typ.)
- Build in Current Limitting Circuit
- Low Drop Out Voltage : $|V_{IN}-V_{OUT}|=1.8V$
- High Output Current : I_{OUT}=200mA(Max.)
- Output Current Up to 5A Can be Supplied by Connecting External Transistor.
- The TA7089P is Easily Mounted on a Printed Circuit Board, and is Provided with 14 Pin Output, 7 Pin GND and 1 Pin Input for Application as a Power Supply for Digital IC.

Unit in mm



Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.14 leads.

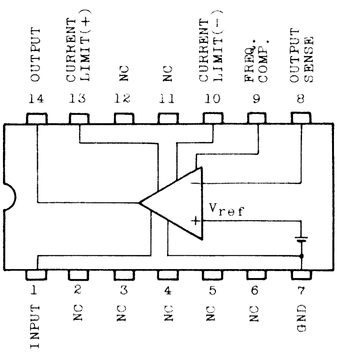
JEDEC	—
TOSHIBA	5−21D

MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Input Voltage	V_{IN}	35	V
Terminal Voltage 8	V_8	7	V
Output Current	I_{OUT}	-200	mA
Power Dissipation	P_D	600	mW
Operating Temperature	Topr	-30 ~ 75	°C
Storage Temperature	Tstg	-55 ~ 125	°C

PIN CONNECTION

TOP VIEW



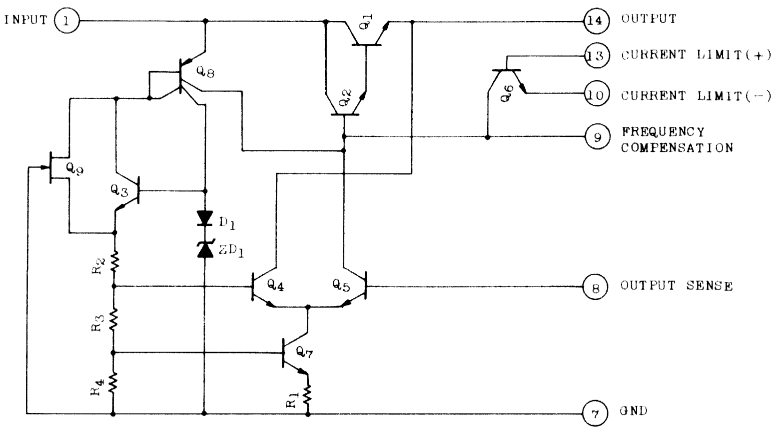
TA7089P

ELECTRICAL CHARACTERISTICS (Ta=25°C)

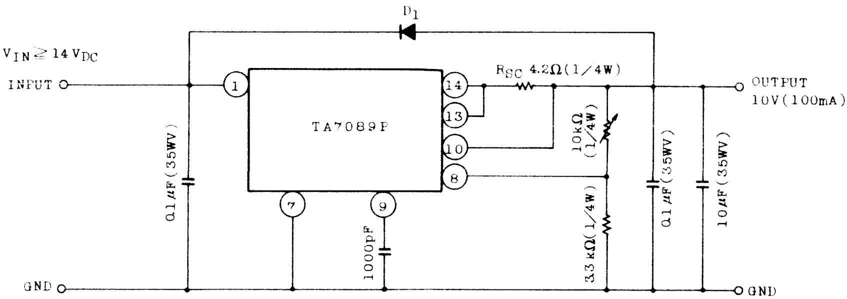
CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage	V_{IN}	1	-	7	-	35	V
Output Voltage	V_{OUT}	1	$7 < V_{IN} < 35V$ $I_{OUT}=50mA$	3.3	0	33	V
Drop Output Voltage	$\vert V_{IN}-V_{OUT}\vert$	1	$R_{SC}=0$, $I_{OUT}=200mA$	2.0	1.8	-	V
Reference, Voltage	V_{ref}	1	$7 < V_{IN} < 35V$ $I_{OUT}=0mA$	2.7	3.0	3.3	V
Bias Current	I_B	1	$7 < V_{IN} < 35V$ $V_{OUT}=0mA$	1.5	3	6	mA
Ripple Rejection	RR	2	$V_{IN}=14V$, f=1kHz $V_{OUT}=10V$, $I_{OUT}=50mA$	40	48	-	dB
Output Voltage Temperature Coefficient	TC_{VO}	1	-	-	±0.02	-	%/°C
Output Current	I_{OUT}	1	-	-	-	-200	mA
Output Impedance	Z_O	3	$V_{IN}=14V$, f=1kHz $V_{OUT}=10V$, $I_{OUT}=50mA$	-	40	150	mΩ
Input Regulation	Reg·line	1	$I_{OUT}=50mA$ $15 < V_{IN} < 35V$	-	-	300	mV
Load Regulation	Reg·load	1	$V_{IN}=15V$ $50 < I_{OUT} < 200mA$	-	-	60	mV

TA7089P

EQUIVALENT CIRCUIT



STANDARD APPLICATION CIRCUIT (10V, -100mA)



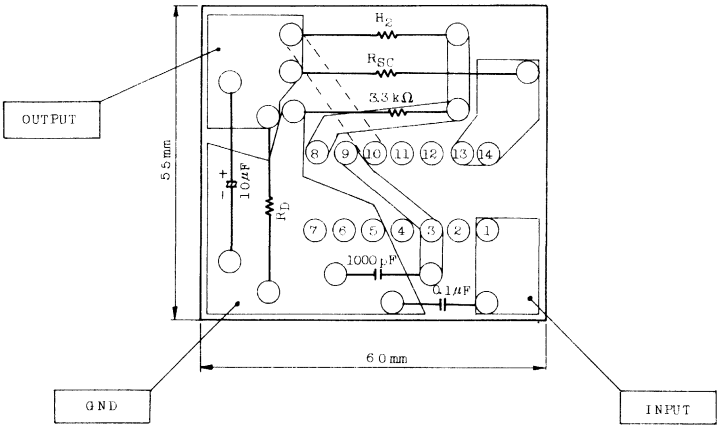
Note : IC Protecting Diode

When the surge voltage is applied to the IC output or when V_{IN}^{+} becomes more than V_{OUT}^{+}(C_{IN} V_{OUT}) at times of power ON or OFF.
It is required to cannot high speed diodes between input and output terminals.

TA7089P

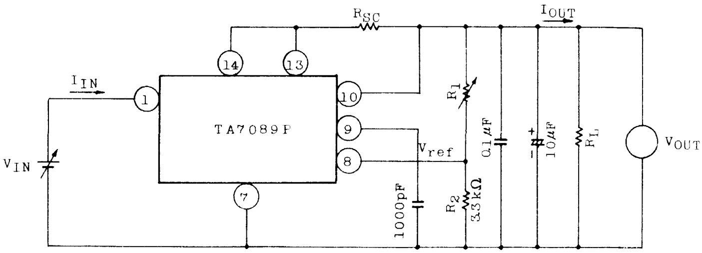
STANDARD PRINT BOARD

PATTERN



TEST CIRCUIT

1. V_{IN}, V_{OUT}, $|V_{IN}-V_{OUT}|$, I_{OUT}, I_B, V_{ref}, Reg·line, Reg·load, TC_{VO}

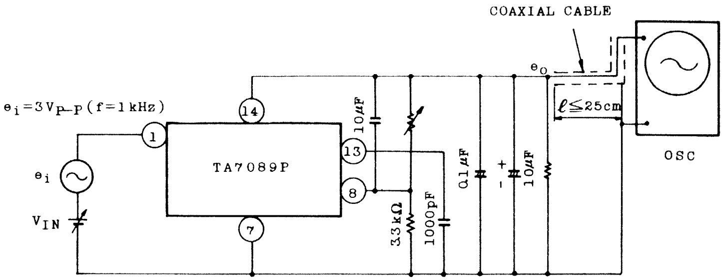


$$V_{OUT} = \frac{R_1+R_2}{R_2} \times V_{ref}$$

$$I_B = I_{IN} - I_{OUT}$$

$$TC_{VO} = \frac{V_{OUT}(75°C) - V_{OUT}(-30°C)}{V_{OUT}(25°C) \times 105} \times 100\ (\%/°C)$$

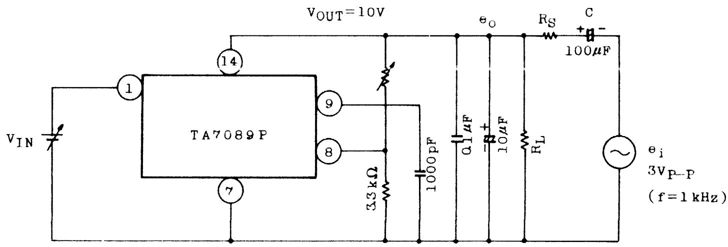
2. RR



Ripple Rejection

$$RR = 20\ \ell og\ 10 \left(\frac{e_i}{e_o}\right) \quad (dB)$$

3. Z_O



Z_O Calculation Method

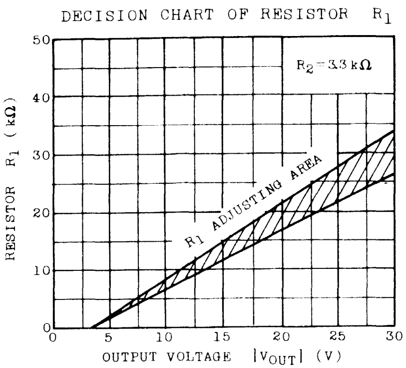
$$e_O = \frac{e_i}{R_S+Z_O} \cdot Z_O$$

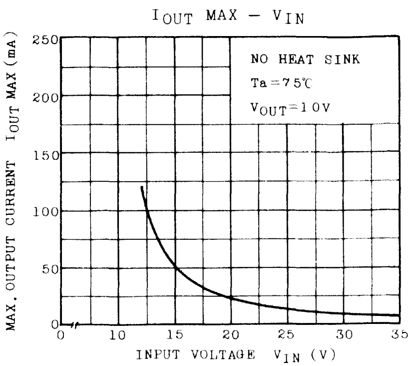
$$R_S \gg Z_O$$

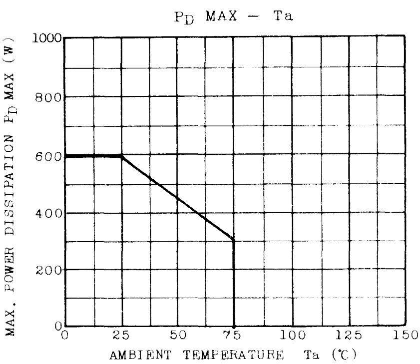
$$e_O = \frac{e_i}{R_S} \cdot Z_O$$

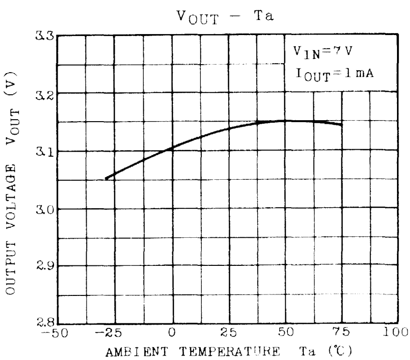
Therefore, $Z_O = \frac{e_O}{e_i} \cdot R_S \ (\Omega)$

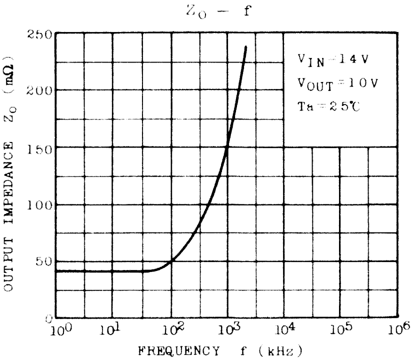
TA7089P

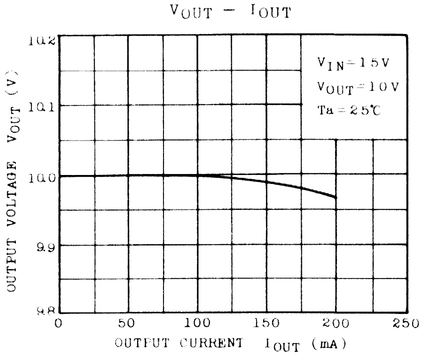

DECISION CHART OF RESISTOR R1
R2=3.3kΩ
R1 ADJUSTING AREA
RESISTOR R1 (kΩ)
OUTPUT VOLTAGE |VOUT| (V)
0
10
20
30
40
50
0
5
10
15
20
25
30

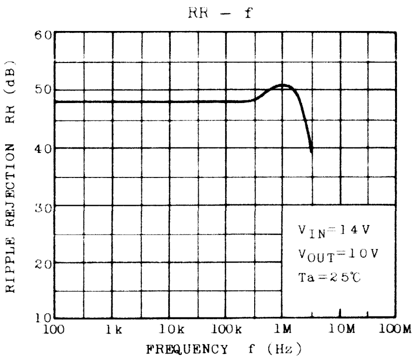

IOUT MAX — VIN
NO HEAT SINK
Ta=75℃
VOUT=10V
MAX. OUTPUT CURRENT IOUT MAX (mA)
INPUT VOLTAGE VIN (V)
0
50
100
150
200
250
0
10
15
20
25
30
35

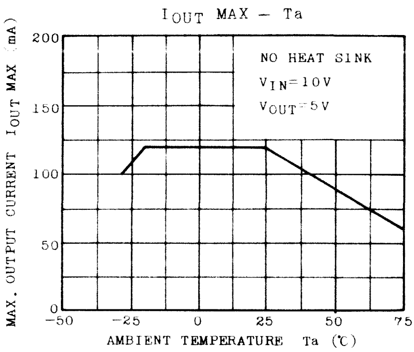

PD MAX — Ta
MAX. POWER DISSIPATION PD MAX (W)
AMBIENT TEMPERATURE Ta (℃)
0
200
400
600
800
1000
0
25
50
75
100
125
150


VOUT — Ta
VIN=7V
IOUT=1mA
OUTPUT VOLTAGE VOUT (V)
AMBIENT TEMPERATURE Ta (℃)
2.8
2.9
3.0
3.1
3.2
3.3
−50
−25
0
25
50
75
100


Z_O – f
V_{IN}=14V
V_{OUT}=10V
Ta=25℃
OUTPUT IMPEDANCE Z_O (mΩ)
250
200
150
100
50
0
10^0 10^1 10^2 10^3 10^4 10^5 10^6
FREQUENCY f (kHz)

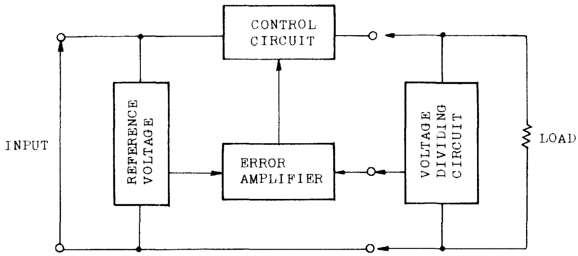

V_{OUT} – I_{OUT}
V_{IN}=15V
V_{OUT}=10V
Ta=25℃
OUTPUT VOLTAGE V_{OUT} (V)
10.2
10.1
10.0
9.9
9.8
0 50 100 150 200 250
OUTPUT CURRENT I_{OUT} (mA)


RR – f
V_{IN}=14V
V_{OUT}=10V
Ta=25℃
RIPPLE REJECTION RR (dB)
60
50
40
30
20
10
100 1k 10k 100k 1M 10M 100M
FREQUENCY f (Hz)


I_{OUT} MAX – Ta
NO HEAT SINK
V_{IN}=10V
V_{OUT}=5V
MAX. OUTPUT CURRENT I_{OUT} MAX (mA)
200
150
100
50
0
−50 −25 0 25 50 75
AMBIENT TEMPERATURE Ta (℃)

TA7089P

BLOCK DIAGRAM

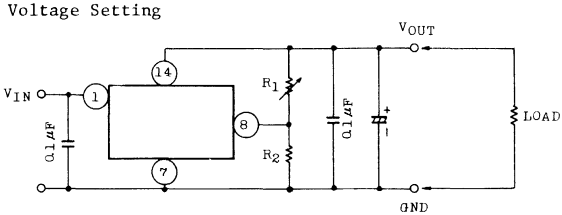


METHOD OF USE AND GENERAL PRECAUTIONS

1. Input Voltage Range

   The TA7089P can be used at 7 ~ 35V.

2. Output Voltage Setting



Output voltage is set by resistor R_1 (See resistor-output voltage characteristic diagram.)

If $\quad V_{OUT} = \dfrac{V_{ref}\ (R_1+R_2)}{R_2}$

Where, $V_{ref}=3V$

$R_2=3.3k\Omega$

Output voltage is

$$\begin{cases} V_{OUT}=0.9\times 10^{-3}\times R_1+3(V) \\ V_{IN}>V_{OUT}+2 \end{cases}$$

Output voltage setting range is 3.3 ~ 33V.

3. Power Dissipation

Internal power dissipation P_D in IC at normal operation is

$$P_D = V_{IN} \times I_B + (V_{IN} - V_{OUT}) \times I_{OUT}$$

Where, I_B : Bias Current, V_{IN} : Input Voltage, V_{OUT} : Output Voltage, I_{OUT} : Output Current

Power dissipation at output shorted condition.

$$P_D = (I_{SC} + I_B) V_{IN}$$

Max. Power dissipation P_D MAX. must be as follows :

$$P_D \text{ MAX.} < \frac{T_j \text{ MAX} - Ta}{R_{th}}$$

Where, T_j MAX. ; Junction Temperature

Ta ; Ambient Temperature

R_{th} ; Thermal Resistance

T_j MAX. and R_{th} of the TA7089P are ;

T_j MAX. = 125°C

R_{th}=165°C/W (Free Air)

4. Rang of Output Current

Rang of output current is 0 ~ 200mA.

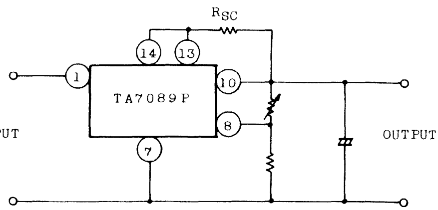
When output current is above 200mA, use external transistors.

(See Application circuits.)

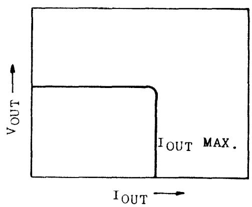
5. Control of Output Current

The TA7089P has a build-in output current limitting transistor and is therefore capable of constant current and fold back current limitting.

The constant current is limited as shown in the following diagrams.



OVER CURRENT PROTECTIVE CHARACTERISTICS

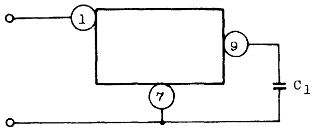


TA7089P

Output current is limited at a point where voltage in RSC drops to voltage between the transistor base and emitter V_{BE} (about 0.65V at T_j=25°C)

$$R_{SC} = \frac{V_{BE}}{I_{OUT\ MAX.}} \qquad \text{Where,} \quad V_{BE} \doteqdot V_{BE}(T_j=25°C) - 2 \times 10^{-3}\ (T_j-25)$$

6. Phase Compensating Capacitor



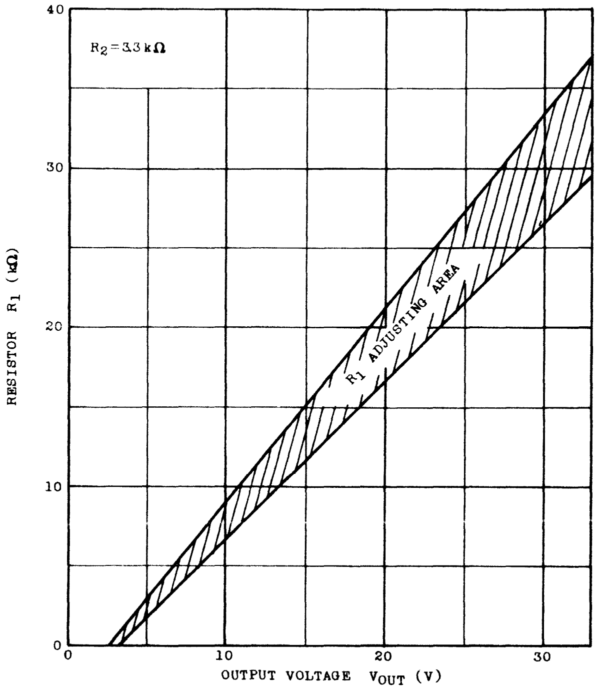
Select a capacitor having capacity 0.1μF-1000pF according to the external wiring conditions. Normally, use a capacitor at 1000pF.

7. Output Capacitors

Output capacitors of 10μF and 0.1μF shall be mounted parallelly.

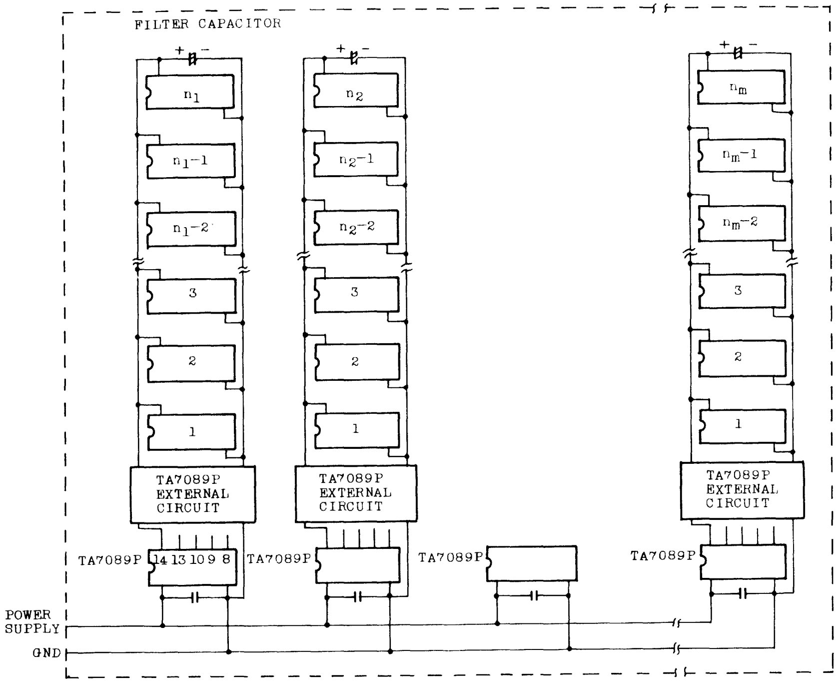
TA7089P

DECISION CHART OF RESISTOR R_1



TA7089P

BASIC EXAMPLE OF 10μF MOUNTING OF TA7089P ON PRINTED CIRCUIT BOARD
(LOCAL REGULATOR APPLICATION)



ADVANTAGES

. Mutual effect between raws can be ignored.

. Adjustment is simple as malfunction due to noise is reduced.

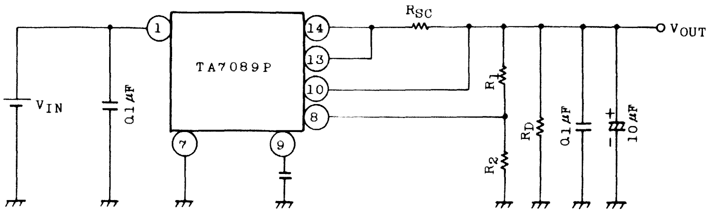
. Pattern design is simple as the pin arrangement is 14 pins for output, 7 pins for GND and 1 pin for input.

. THL. IC, TTL. IC and other supply voltages can be incorporated into a same printed circuit board.

TA7089P

APPLICATION (1)

1. Circuit Diagram



2. Decision of Circuit Constant

Circuit specification

. Output Voltage $V_{OUT}=6V$

. Max. Output Current I_{OUT} MAX.=50mA

. Output Limitting Current $I_{SC}=70mA$

Decision of voltage dividing resistors R_1 and R_2

A resistor of 3.3kΩ is used as R_2 by considering current balance of a differential amplifier.

R_1 is obtained from the following expression or the resistor R_1 set-up table.

$$V_{OUT} = \frac{R_1+R_2}{R_2} \times V_{ref}$$

V_{ref} is in the range of 2.7~3.3V from the specification.

When R_1 is obtained through calculation according to the above, it is $2.7k\Omega \leq R_1 \leq 4.4k\Omega$

Further, 3~4kΩ is obtained from the R_1 set up table.

Therefore, Resistor R_1 would be 3kΩ (fixed) + 1kΩ (variable resistor).

Decision of R_{SC}.

Current limitting resistor RSC value is obtained from the following expression :

$V_{BE} = R_{SC} \times I_{SC}$

V_{BE} : Base to emitter voltage of an internal current limitting transistor.

TA7089P

A value at $T=T_j$ is applied.
Assuming that a value of V_{BE} (at $T_j=125°C$) is 0.45V, R_{SC} is 6.4Ω when $I_{SC}=70mA$ is substituted.

Decision of Min. Input Voltage

Min. input voltage V_{IN} MIN. which is required to operate this circuit is

V_{IN} MIN.$=V_{OUT}+|V_{IN}-V_{OUT}|+V_R$

V_R : Voltage between R_{SC}

Where, $V_{OUT}=6V$

$|V_{IN}-V_{OUT}|=2V$ (from the Electrical characteristic table)

$V_R=0.65V$

Therfore, V_{IN} MIN.=8.65V

Decision of R_D

R_D is dummy resistor used to flow current constantly in order to operate the circuit stability.
Required current is approximately 3mA.

$$R_D = \frac{V_{OUT}}{3mA} \doteqdot 1.8k\Omega$$

Calculation of P_D

At the normal condition, max. power dissipation of IC is obtained from the following expression :

$$P_D=V_{IN}\times I_B+(V_{IN}-V_{OUT})\times I_{OUT}$$

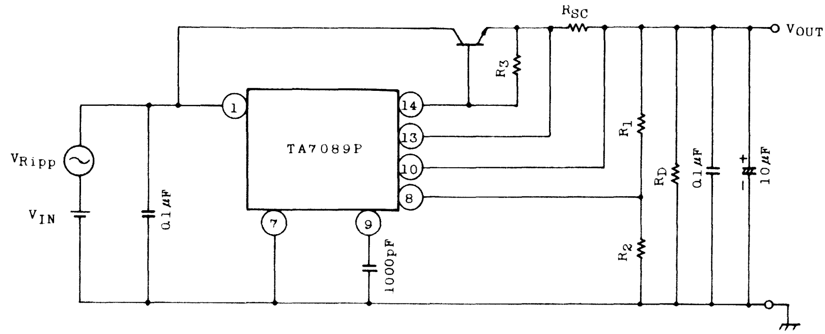
Power dissipation at load shorted condition is obtained from the following expression :

$$P_D=V_{IN}\times I_B+(V_{IN}-V_R)\times I_{SC}$$

Designing should be made carefully by calculating power dissipation at time of load shorted, input voltage and transformers so that P_D MAX. is not exceeded.

APPLICATION (2) CURRENT BOOST CIRCUIT EXAMPLE

1. CIRCUIT



2. Decision of Circuit Constants

Circuit Specification

. Output Voltage V_{OUT} 5V

. Max. Output Current I_{OUT} MAX. 1A

. Current Limitting Protection Circuit

. Decision of Voltage Dividing Resistors R_1 and R_2

A resistor of 3.3k is used as R_2 by considering current balance of a differential amplifier.

R_1 is obtained from the following expression :

$$V_{OUT} = \frac{R_1+R_2}{R_2} \times V_{ref}$$

When the resistor R_1 setting table (2) is used,

$$R_1 = 1.5k\Omega \sim 3k\Omega$$

Therefore, R_1 would be 1.5kΩ (fixed) + 2kΩ (variable).

. Decision of R_{SC}

$$V_{BE} = R_{SC} \times I_{SC}$$

Assuming that

I_{SC}=1.2A

V_{BE}=0.65V

$$R_{SC} = \frac{V_{BE}}{I_{SC}} = \frac{0.45V\ (T_j=125°C)}{1.2} = 0.4\ (\Omega)$$

TA7089P

Rated capacity is

$0.65V \times 1.2A = 0.78$ (W)

$R_{SC}=0.4\Omega$ (1W)

. Decision of Min. Input Voltage

Obtaind Min. input voltage of the circuit.

$$V_{IN}\ MIN = V_{OUT} + |V_{IN} - V_{OUT}| + V_{BE} + V_R$$

V_R : Voltage between R_{SC}

when, $V_{OUT}, |V_{IN} - V_{OUT}|$, V_{BE}, V_R

expression, $V_{IN}\ MIN = 5.0 + 2.0 + 0.7 + 0.6$

$= 8.3$ (V)

Further, as the catalog standard is 7V or above,

$V_{IN}\ MIN = 8.3$ (V)

. Decision of R_3

Resistor R_3 is to be inserted for stabilizing the circuit and several mA would be sufficient.

When the circuit is designed by assuming that current is 5mA.

$$R_3 = \frac{V_{BE}}{5mA} = \frac{0.7V}{5mA} \doteqdot 150\ (\Omega)$$

. Decision of R_D

Resistor R_D is used to apply dummy current and functions to stabilize the circuit together with R_3.

1 ~ 10mA is generally accepted. The design is made here at 5mA.

$$R_D = \frac{V_{OUT}}{I_D} = \frac{5V}{5mA} = 1\ (k\Omega)$$

Summary

R_2	3.3kΩ
R_1	1.5kΩ (fixed) + 2kΩ (variable)
R_{SC}	0.4Ω (1W)
R_3	150Ω
R_D	1kΩ
V_{IN} MIN.	8.3V

3. Parastic Oscillation Prevention

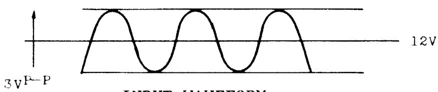
To prevent a parastic oscillation, insert a capacitor of about 0.1µF into the input and output sides. It would be effective when the capacitor is insert as close as to IC terminals.

4. Example of Output Voltage Ripple Value Calculation

Assuming that input ripple voltage is 3 V_{p-p} AC,

$V_{IN} = 10V_{DC} + 3V_{p-p}$ AC

However, actual mean value of full load input voltage when voltage fluctuation at the transformer primary side is considered is 12V DC.



INPUT WAVEFORM

Obtain output ripple voltage.

As Reg. in is min. 40(dB) from the standard data table,

(Output ripple voltage) = 30mV_{p-p} AC.

5. Selection of Power Transistor

Full Load Input Voltage	12V (AVG)
Output Voltage	5V
Output Current	1A

When P_D MAX. is obtained from the above data,

P_D MAX = (12-5) × 1

= 7 (W)

However, when power dissipation resulted from output short is calculated.

P_D MAX = 12 × 1.2 = 14.4 (W)

2SD867 (or equivalent) is selected this time from TOSHIBA SEMICONDUCTOR HAND BOOK.

TA7089P

6. Design of Heat Sink

1) Design of power transistor radiation

From the 2SD 867 data table (TOSHIBA SEMICONDUCTOR HAND BOOK)

$$R_{th(j-c)} = \frac{150-25}{100} = 1.25°C/W$$

Therefore, $R_{th(j-a)}=1.25+1.0+R_{th(f)}$

(It is assumed that $R_{th(s)}+R_{th(c)}=1.0°C/W$)

P_D MAX = 14.4W
T_j MAX = 150°C
Ta=60°C (Including temperature rise in device)

From the above data,

$$R_{th(j-a)} = \frac{T_j\ MAX - Ta}{P_D\ MAX} = \frac{150-60}{14.4} = 6.2°C/W$$

Accordingly, thermal resistance required for a heat sink is,

$$\begin{aligned} R_{th(f)} &= R_{th(j-a)} - R_{th(j-c)} - R_{th(s)} - R_{th(c)} \\ &= 6.2 - 1.25 - 1.0 \\ &= 3.95°C/W \end{aligned}$$

When an $A\ell$ heat sink is used, size required can be seen as follows from TOSHIBA SEMICONDUCTOR HAND BOOK :

100mm × 170mm × 2mm

Further, in actual designing it is a general practice to derate T_j MAX taking reliability into consideration.

2) Design of IC Heat Sinking

Max. power consumed in IC is obtained from the following expression :

$$P_D\ MAX = (V_{IN}\ MAX-V_{BE(1)}) \times \left(\frac{I_{SC}-V_{BE(2)}/R_3}{h_{FE(MIN)}} + \frac{V_{BE(2)}}{R_3} + I_B\ MAX\right)$$

Assuming that

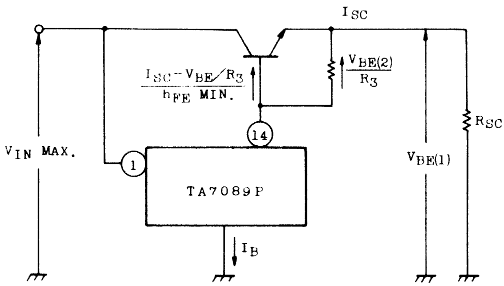
$V_{BE(1)}$: V_{BE} of current limitting internal transistor = 0.65V

$V_{BE(2)}$: V_{BE} of power transistor = 0.65V

h_{FE} MIN : Min. value of h_{FE} of power transistor (at $I_C=I_{SC}$) $\doteqdot$ 40

I_B MAX : Max. value of bias current of TA7089P = 6mA

P_D MAX is above 504mW.



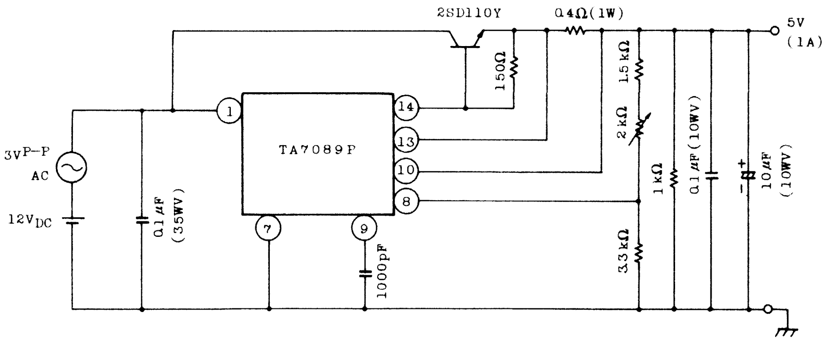
7. Application

Specification

V_{IN}	$12V_{DC}$ + $3V^{P-P}{}_{AC}$
V_{OUT}	$5V_{DC}$ + $30mV^{P-P}{}_{AC}$
I_L MAX	1.2A

Current limitting protection circuit

Example 1. Current Boost Circuit

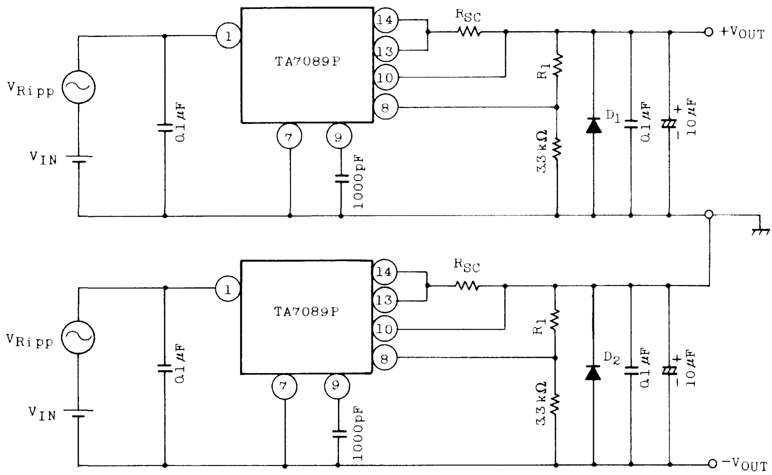


2SD876 Heat Sink ($R_{th(f)}$ = 3.95°C/W)

100 × 170 × 2mm Aℓ

TA7089P

Example 2. Positive and Negative Power Supplied



Use diodes having less forward voltage drop for D_1 and D_2.

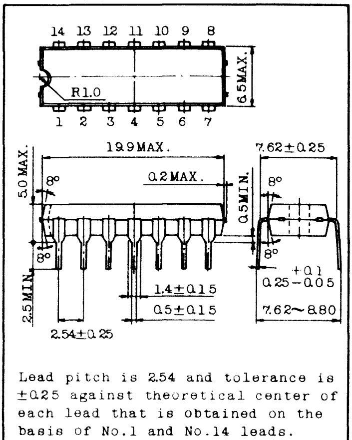
BIPOLAR LINEAR INTEGRATED CIRCUIT
SILICON MONOLITHIC

TA7179P

DUAL ±15V TRACKING REGULATOR

. Output Voltage of ±15V with Tracking Characteristic.
. Excellent Input and Load Regulation :
  Reg. line=5mV(Typ.) (V_{IN}=18 ~ 30V)
  Reg. Load=5mV(Typ.) (I_{OUT}=0 ~ 50mA)
. High Ripple Rejection : RR=75dB(Typ.)
. Output Current Up to 100mA (Max.)
. Excellent Temperature Stability :
  TC_{VO}=0.007%/deg.(Typ.)
. Designed Especially for Use Operational Amplifier Power Regulator.
. Built-in Overcurrent Protective Circuit.

Unit in mm



Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.14 leads.

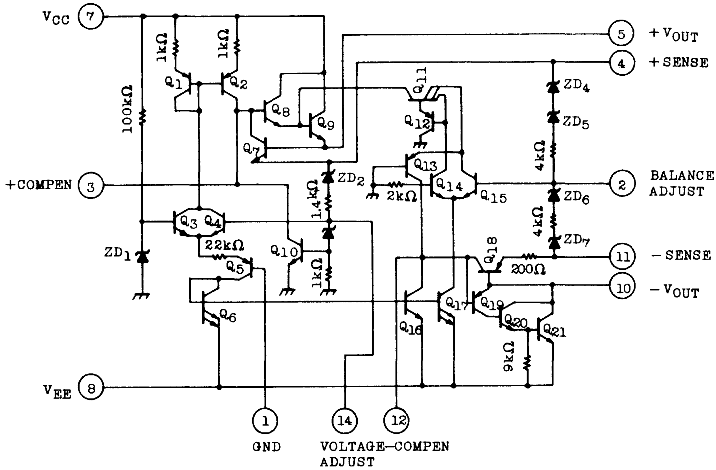
JEDEC	—
東芝	5-21D

MAXIMUM RATINGS (Ta=25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Input Voltage	$+V_{IN}$	30	V
	$-V_{IN}$	-30	
Output Current	$+I_{OUT}$	-100	mA
	$-I_{OUT}$	+100	
Power Dissipation	P_D	625	mW
Operating Temperature	T_{opr}	-30 ~ 75	°C
Storage Temperature	T_{stg}	-50 ~ 150	°C

TA7179P

EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS

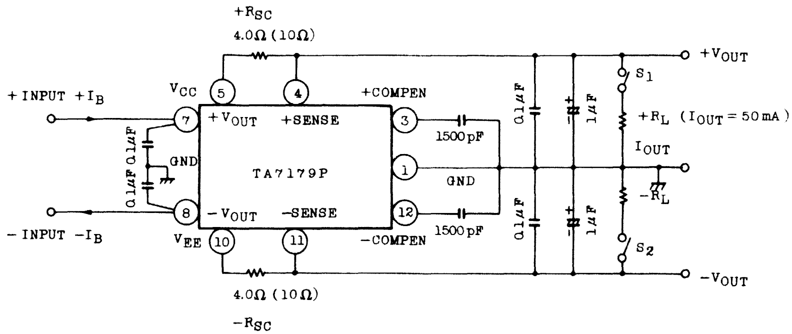
(Unless otherwise specified, V_{CC}=20V, V_{EE}=−20V, $\pm I_{OUT}$=0, R_{SC}^{+}=R_{SC}^{-}=4Ω, Ta=25°C)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Voltage	V_{OUT}	1	-	±14.5	±15.0	±15.5	V
Drop Output Voltage	$\lvert V_{IN}-V_{OUT}\rvert$	-	I_{OUT}=100mA	2.0	-	-	V
Output Voltage Balance	V_{BAL}	-	-	-	±50	±150	mV
Input Regulation	Reg·line	1	V_{IN}=18 ~ 30V	-	5	-	mV
Load Regulation	Reg·load	1	I_{OUT}=0 ~ 50mA	-	5	-	mV
Output Voltage Variable Range	V_{OUT}-R	-	-	±8.0	-	±2.0	V
Ripple Rejection	RR	2	f=120Hz 2V_{p-p}	-	75	-	dB
Output Voltage Temperature Coefficient	TC_{VO}	1	-	-	0.007	-	%/deg
Output Short-Circuit Current	I_{SC}	1	R_{SC}=10Ω	40	60	80	mA
Positive Stand-by Current	I_B^{+}	1	-	-	2.4	4.0	mA
Negative Stand-by Current	I_B^{-}	1	-	-	1.0	3.0	mA
Long-Time Stability	$\Delta V_{OUT}/\Delta t$	1	-	-	0.2	-	%/1000 hr

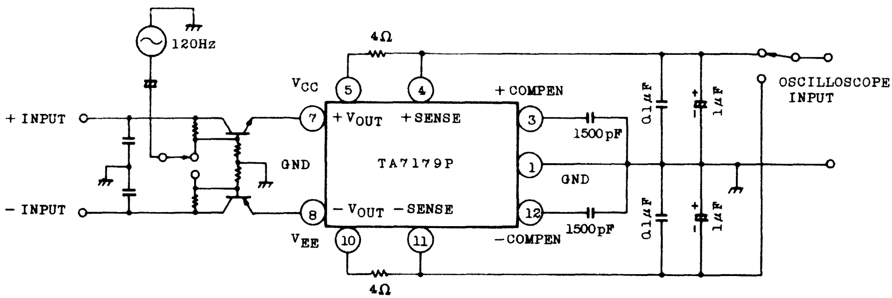
TA7179P

TEST CIRCUIT

1. V_{OUT}, V_{BAL}, Reg·line, Reg·load, TC_{VO}, I_{SC}, $I_B^+ \cdot I_B^-$, $\Delta V_{OUT}/\Delta t$



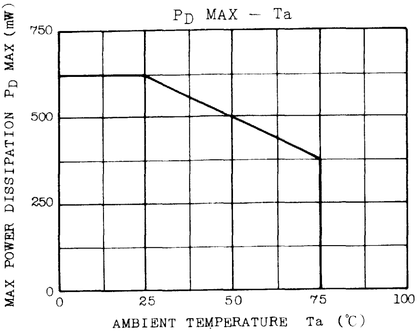
2. RR



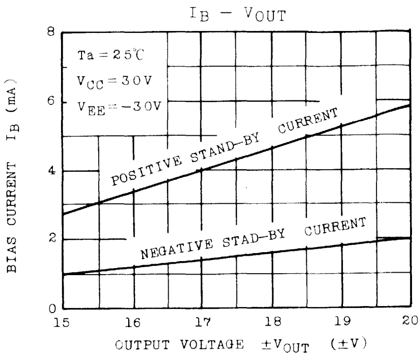
V_{CC}=+20V, V_{EE}=-20V, e_i=2V_{P-P} (f=120Hz)

$$RR = 20\ell og \frac{e_o}{e_i} \quad (dB)$$

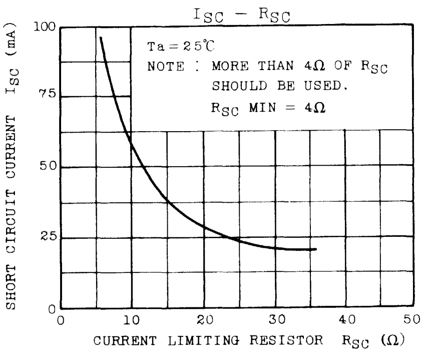
TA7179P



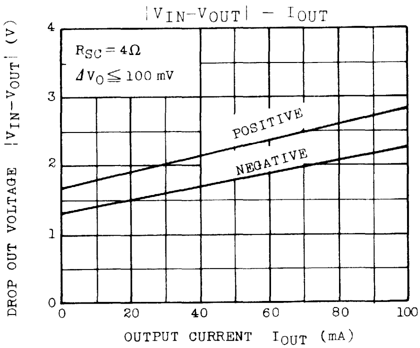
PD MAX – Ta
MAX POWER DISSIPATION PD MAX (mW)
750
500
250
0
0
25
50
75
100
AMBIENT TEMPERATURE Ta (℃)



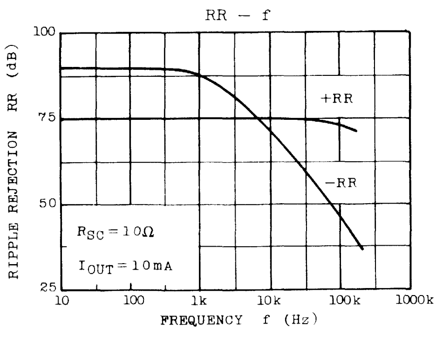
IB – VOUT
Ta = 25℃
VCC = 30V
VEE = −30V
POSITIVE STAND-BY CURRENT
NEGATIVE STAD-BY CURRENT
BIAS CURRENT IB (mA)
8
6
4
2
0
15
16
17
18
19
20
OUTPUT VOLTAGE ±VOUT (±V)



ISC – RSC
Ta = 25℃
NOTE : MORE THAN 4Ω OF RSC SHOULD BE USED.
RSC MIN = 4Ω
SHORT CIRCUIT CURRENT ISC (mA)
100
75
50
25
0
0
10
20
30
40
50
CURRENT LIMITING RESISTOR RSC (Ω)



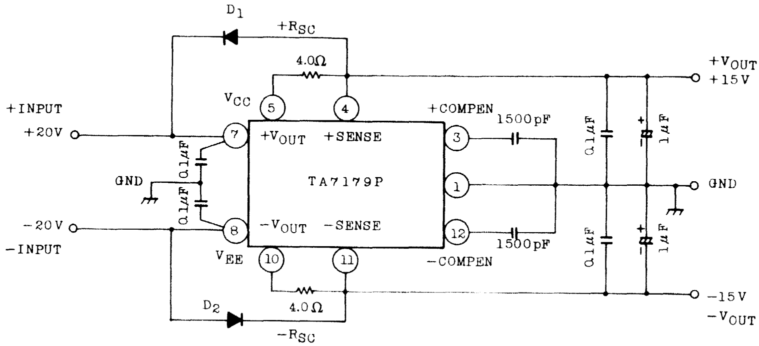
|VIN−VOUT| – IOUT
RSC = 4Ω
ΔVO ≦ 100 mV
POSITIVE
NEGATIVE
DROP OUT VOLTAGE |VIN−VOUT| (V)
4
3
2
1
0
0
20
40
60
80
100
OUTPUT CURRENT IOUT (mA)



RR – f
+RR
−RR
RSC = 10Ω
IOUT = 10mA
RIPPLE REJECTION RR (dB)
100
75
50
25
10
100
1k
10k
100k
1000k
FREQUENCY f (Hz)

APPLICATION CIRCUIT

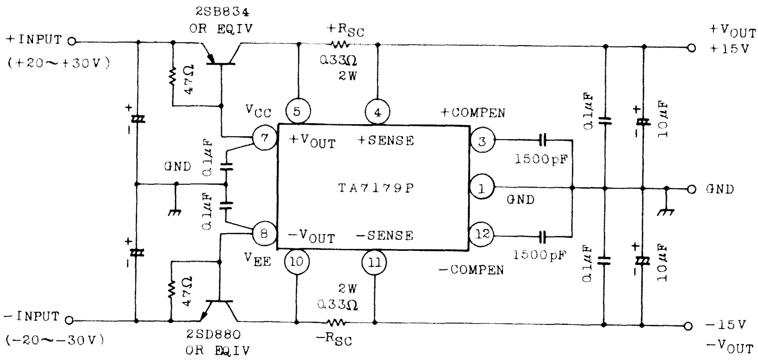
1. STANDARD APPLICATION CIRCUIT



D_1, D_2 : IC protecting diodes

when the surge voltage is applied to the IC output or when V_{IN}^+ becomes less than V_{OUT}^+ ($V_{IN}^- > V_{OUT}^-$) at time of power ON or OFF, connect a high speed switching diodes for circuit protection.

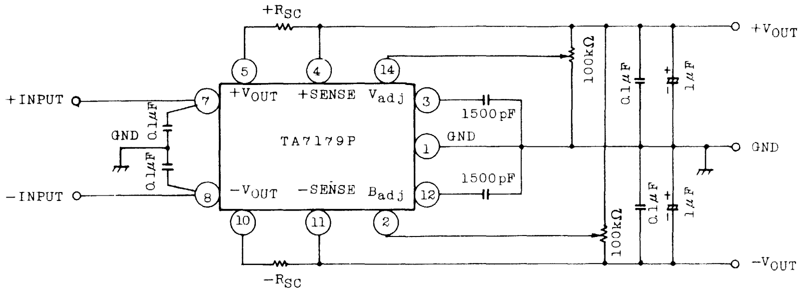
2. CURRENT BOOST CIRCUIT·······±1.5A Regulator



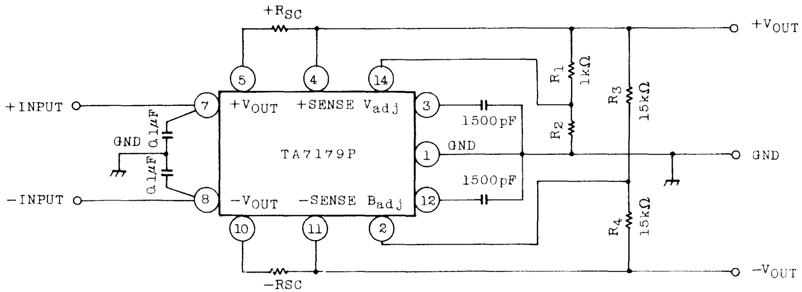
Pay attention to heat sinking design.

TA7179P

3. VOLTAGE AND BALENCE SET-UP CIRCUIT



4. OUTPUT VOLTAGE CHANGING CIRCUIT



Output voltage of the TA7179P can be changed to ±8.0V by connecting a resistor of R_2. For the relationship between output voltage and R_2 see table shown below.

$\pm V_{OUT}$ (V)	R_2 (kΩ)
14.0	1.2
12.0	1.8
10.0	3.5
8.0	∞

TA7179P

APPLICATION NOTE

1. GENERAL DESCRIPTION

When a general purpose regulator IC is used as a power supply for OP AMP, 2 pieces of IC, each of which has positive or negative output voltage of +15V or -15V, are required.

If 2 pieces of IC having positive or negative output voltage are used, the latch-up design at the positive power supply side becomes complicated and therefore, use of these 2 ICs is not desirable. Further, a circuit using OP AMP generally demands high precision in many cases, and various excellent characteristics such as excellent temperature characteristic, excellent stability against fluctuation in supply voltage as well as fluctuation in load and the like are demanded to its power circuit.

There is SVRR (SUPPLY VOLTAGE REJECTION RATIO) for OP AMP against fluctuation in supply voltage, which specifies occurrence of OFF SET resulted from supply voltage fluctuation.

The TA7179P is the optimum monolithic IC as a power supply for OP AMP with excellent temperature stability input and load regulation, and its positive and negative output voltage have tracking characteristic (characteristic in which positive and negative voltage fluctuate symmetrically against 0 level; that is, output current at the positive side only increases and output voltage at the negative side drops following drop in output voltage at the positive side).

As the TA7179P has tracking characteristic, even when an absolute value of output voltage fluctuates, frequencies of OFF SET of OP AMP resulted from fluctuation in output voltage decrease.

The TA7179P is a regulator IC used for OP AMP, having such features as high ripple compression characteristic, a built-in overcurrent protective circuit and high output current (100mA) in addition to these characteristics.

Further, the range of working supply voltage of OP AMP is ±5 ~ 18V although it is normally operated at ±15V.

The TA7179P has been so designed that its output voltages other than ±15V can be obtained through simple external arrangement.

TA7179P

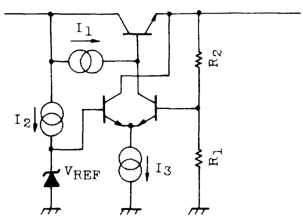
2. CIRCUIT OPERATION

1) Tracking Regulator

On a general regulator, an output transistor is controlled by comparing voltage obtained by dividing V_{OUT} according to resistance ratio between R_1 and R_2 with reference voltage generated by a reference voltage generating circuit in the regulator as shown in Fig. 1.

However, even when 2 power supplies for positive and negative output voltages are provided by using 2 regulator ICs, they can only control respective output voltages independently and have no tracking characteristic. So, when either one of the positive and negative power supplies is provided with an independent control mechanism and + and - output voltages are divided by high precision equal resistors as shown in Fig. 2, and output voltages are controlled by comparing voltage at the divided middle point with GND potential, tracking characteristic is obtained.

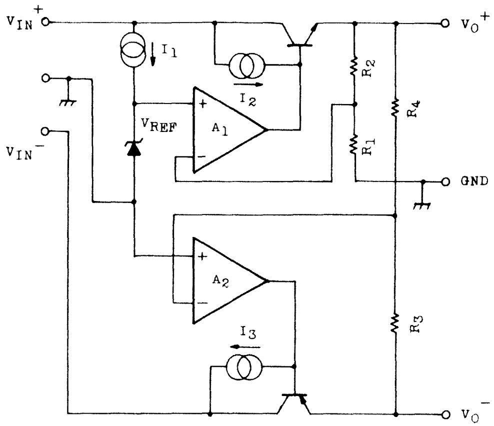
In Fig. 2, the positive power supply side is controlled independently with the negative power supply side followed the positive power supply side but it is also possible to control the negative power supply side but it is also possible to control the negative power supply side and have the positive power supply side follow the negative power supply side.



$$V_{OUT}=V_{REF}\cdot\frac{R_1+R_2}{R_1}$$

Fig. 1

TA7179P



$V_O^{+} = V_{REF} \cdot \frac{R_1+R_2}{R_1}$

R_3 and R_4 are high precision equal resistors.

Fig. 2

2) Internal Configuration

One of the characteristics required for the tracking regulator is balance of output voltages. Balance in output voltages from positive and negative power supplies is virtually decided by relative accuracy of resistors R_3 and R_4 in Fig. 2, which divide positive and negative output voltages.
The TA7179P uses not only resistors but also zener diodes for dividing output voltages.
Further, the circuit is so designed that the positive power supply side is controlled independently and the negative power supply side follows the positive power supply side.
The simplified internal circuit is shown in Fig. 3.

TA7179P

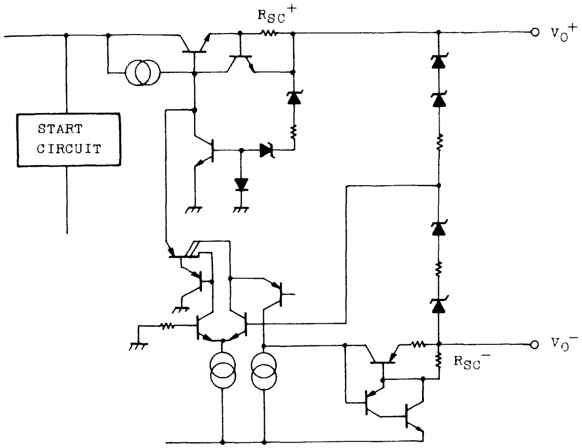


Fig. 3

3. PRECAUTIONS FOR USE

1) Setting Output Voltage

Output voltage of the TA7179P is fixed at ±15V but can be varied by connecting resistors externally.

Examples of the circuit are shown in the application circuit examples (3) and (4).

Output voltage V_{OUT} in the circuit example (4) is expressed by the following expression:

$$V_{OUT} = (V_Z+V_{BE})\left(\frac{R1}{R2} + 1\right) + V_{BE}\cdot R1 \ (V) \ \cdots\cdots\cdots\cdots \ 1)$$

where, V_Z = 6.7V±0.1V

V_{BE} = 0.6 ~ 0.7V

R_1 External resistor (1kΩ)

R_2 External resistor

2) Power Dissipation

Power dissipation of the TA7179P is expressed by the following expression:

$$P_D \doteqdot (V_{IN}^{+}-V_O^{+})\cdot I_L^{+}+(|V_{IN}^{-}|-|V_O^{-}|)\cdot|I_L^{-}|+V_{IN}^{+}\cdot I_B^{+}+|V_{IN}^{-}|\cdot|I_B^{-}| \quad \cdots\cdots\cdots 2)$$

where, V_{IN}^{+} : Positive Input Voltage

V_{IN}^{-} : Negative Input Voltage

I_B^{+} : Positive Bias Current

I_B^{-} : Negative Bias Current

Max. power dissipation is 625mW. As P_D increases when output voltage is dropped or input voltage is raised, max. load current decreases as it is restricted by max. power dissipation.

The following are required for the high reliability design:

. If P_D of the TA7179P has a margin when h_{FE} of the output transistor drops at time of current boost?

. When output is shorted, power dissipation may increase and IC can be damaged. If the overcurrent protective circuit is properly set up?

. Derating should be set at about 80%, if possible, so that junction temperature does not exceed T_j MAX of IC even when rise in ambient temperature is taken into consideration.

. When the TA7179P is connected to a printed circuit board, etc., a board pattern area should be provided to improve radiation effect as high as possible.

3) Max. Input Voltage

Max. input voltage of the TA7179P is ±30V. If input voltage exceeds this max. value momentarily, IC can be damaged. When AC input voltage is improperly regulated or when many power supplies are connected at the same time and there is the possibility for fluctuation of input voltage according to state of their loads, zener diodes should be connected parallelly to the input terminals of IC.

4) Surge Protection

As the input and output voltage terminal lines tend to be extended, surge voltage may be applied to them. It may possibly be applied to not only these lines but also GND of a device. If there is any high-tension circuit, surge absorbing diodes should be connected to terminals to which surge voltage may possibly applied.

5) Input and Output Capacitors

In order to prevent parasitic oscillation which is caused by feedback through the input as well as output lines, capacitors of about 0.1μ should be connected to the input and output terminals of the TA7179P.

It is necessary to connect these capacitors close to the terminals of this IC.

Further, this also applies to phase compensating capacitors. As optimum capacitor values vary depending upon wiring state, wiring should be properly adjusted so that optimum capacitor values can be obtained.

BIPOLAR LINEAR INTEGRATED CIRCUIT
SILICON MONOLITHIC

TA78005AP～TA78024AP

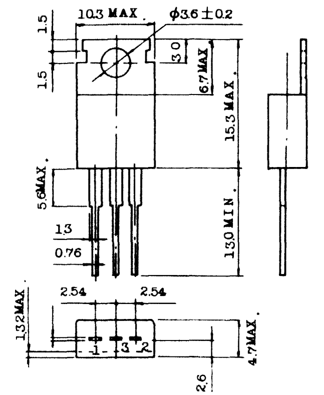
THREE TERMINAL POSITIVE VOLTAGE REGURATORS

5V, *6V, *8V, 9V, 10V, 12V, 15V, *18V, *20V, 24V

* Under development

- Suitable for C-MOS, TTL, the other Digital IC's Power Supply
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Current in excess of 1A

Unit in mm



1. INPUT
2. OUTPUT
3. GND (CASE)

JEDEC	TO-220AB
EIAJ	SC-46
TOSHIBA	5-10A

MOUNTING KIT No. AC75.

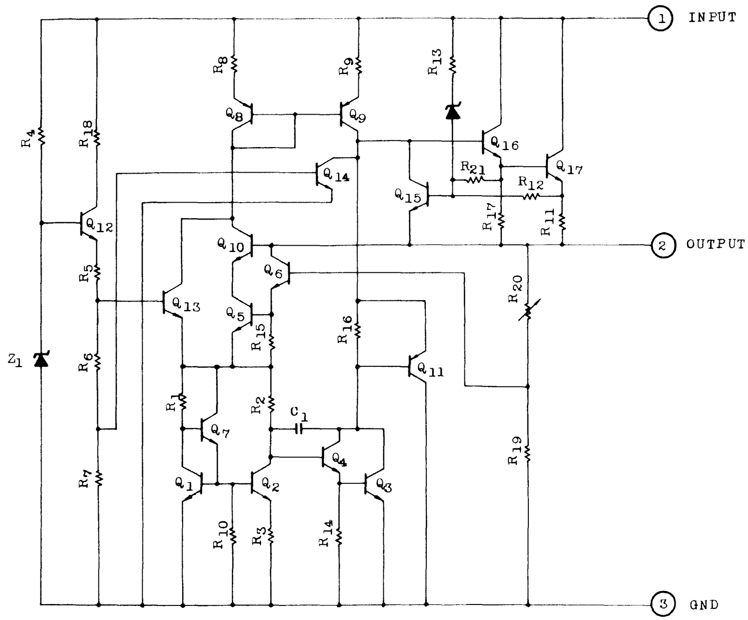
MAXIMUM RATINGS (Ta=25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Input Voltage	TA78005AP ～ TA78015AP	V_{IN}	35	V
	TA78018AP ～ TA78024AP		40	
Power Dissipation (Note)		P_D	20.8	W
Operating Temperature		Topr	-30～75	°C
Storage Temperature		Tstg	-55～150	°C

Note : Tc=25°C

TA78005AP～TA78024AP

EQUIVALENT CIRCUIT



TA78005AP ~ TA78024AP

TA78005AP

ELECTRICAL CHARACTERISTICS (V_{IN}=10V, I_{OUT}=500mA, 0°C≦T_j≦125°C)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Output Voltage	V_{OUT}	1	T_j=25°C, I_{OUT}=100mA		4.8	5.0	5.2	V
Input Regulation	Reg.line	1	T_j=25°C	7.0V≦V_{IN}≦2.5V	-	3	100	mV
				8.0V≦V_{IN}≦12V	-	1	50	
Load Regulation	Reg.load	1	T_j=25°C	5mA≦I_{OUT}≦1.4A	-	15	100	mV
				250mA≦I_{OUT}≦750mA	-	5	50	
Output Voltage	V_{OUT}	1	7.0V≦V_{IN}≦20V 5.0mA≦I_{OUT}≦1.0A, P_O≦15W		4.75	-	5.25	V
Quiescent Current	I_B	1	T_j=25°C, I_{OUT}=5mA		-	4.2	8.0	mA
Quiescent Current Change	ΔI_B	1	7.0V≦V_{IN}≦25V		-	-	1.3	mA
Output Noise Voltage	V_{NO}	1	Ta=25°C, 10Hz≦f≦100kHz I_{OUT}=50mA		-	50	-	μV
Ripple Rejection	RR	1	f=120Hz, 8.0V≦V_{IN}≦18V I_{OUT}=50mA, T_j=25°C		62	78	-	dB
Dropout Voltage	V_D	1	I_{OUT}=1.0A, T_j=25°C		-	2.0	-	V
Short Circuit Current Limit	I_{SC}	1	T_j=25°C		-	1.6	-	A
Average Temperature Coefficient of Output Voltage	T_{CVO}	1	I_{OUT}=5mA, 0°C≦T_j≦125°C		-	-0.6	-	mV/deg

TA78005AP～TA78024AP

TA78006AP

ELECTRICAL CHARACTERISTICS (V_{IN}=11V, I_{OUT}=500mA, $0^{\circ}C \leq T_j \leq 125^{\circ}C$)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Output Voltage	V_{OUT}	1	$T_j=25^{\circ}C$, I_{OUT}=100mA		5.75	6.0	6.25	V
Input Regulation	Reg·line	1	$T_j=25^{\circ}C$	$8.0V \leq V_{IN} \leq 25V$	-	4	120	mV
				$9V \leq V_{IN} \leq 13V$	-	2	60	
Load Regulation	Reg·load	1	$T_j=25^{\circ}C$	$5mA \leq I_{OUT} \leq 1.4A$	-	15	120	mV
				$250mA \leq I_{OUT} \leq 750mA$	-	5	60	
Output Voltage	V_{OUT}	1	$8V \leq V_{IN} \leq 21V$ $5.0mA \leq I_{OUT} \leq 1.0A$, $P_O \leq 15W$		5.7	-	6.3	V
Quiescent Current	I_B	1	$T_j=25^{\circ}C$, I_{OUT}=5mA		-	4.3	8.0	mA
Quiescent Current Change	ΔI_B	1	$8.0V \leq V_{IN} \leq 25V$		-	-	1.3	mA
Output Noise Voltage	V_{NO}	1	$Ta=25^{\circ}C$, $10Hz \leq f \leq 100Hz$ I_{OUT}=50mA		-	55	-	μV
Ripple Rejection	RR	1	f=120Hz, $9V \leq V_{IN} \leq 19V$ I_{OUT}=50mA, $T_j=25^{\circ}C$		61	77	-	dB
Dropout Voltage	V_D	1	I_{OUT}=1.0A, $T_j=25^{\circ}C$		-	2.0	-	V
Short Circuit Current Limit	I_{SC}	1	$T_j=25^{\circ}C$		-	1.5	-	A
Average Temperature Coefficient of Output Voltage	T_{CVO}	1	I_{OUT}=5mA, $0^{\circ}C \leq T_j \leq 125^{\circ}C$		-	-0.7	-	mV/deg

TA78005AP～TA78024AP

TA78008AP

ELECTRICAL CHARACTERISTICS (V_{IN}=14V, I_{OUT}=500mA, $0^{\circ}C \leq T_j \leq 125^{\circ}C$)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Output Voltage	V_{OUT}	1	$T_j=25^{\circ}C$, I_{OUT}=100mA		7.7	8.0	8.3	V
Input Regulation	Reg·line	1	$T_j=25^{\circ}C$	$10.5V \leq V_{IN} \leq 25V$	-	6	160	mV
				$11V \leq V_{IN} \leq 17V$	-	2	80	
Load Regulation	Reg·load	1	$T_j=25^{\circ}C$	$5mA \leq I_{OUT} \leq 1.4A$	-	12	160	mV
				$250mA \leq I_{OUT} \leq 750mA$	-	4	80	
Output Voltage	V_{OUT}	1	$10.5V \leq V_{IN} \leq 23V$ $5.0mA \leq I_{OUT} \leq 1.0A$, $P_O \leq 15W$		7.6	-	8.4	V
Quiescent Current	I_B	1	$T_j=25^{\circ}C$, I_{OUT}=5mA		-	4.3	8.0	mA
Quiescent Current Change	ΔI_B	1	$10.5V \leq V_{IN} \leq 25V$		-	-	1.0	mA
Output Noise Voltage	V_{NO}	1	$T_a=25^{\circ}C$, $10Hz \leq f \leq 100kHz$ I_{OUT}=50mA		-	70	-	μV
Ripple Rejection	RR	1	f=120Hz, $11.5V \leq V_{IN} \leq 21.5V$ I_{OUT}=50mA, $T_j=25^{\circ}C$		58	74	-	dB
Dropout Voltage	V_D	1	I_{OUT}=1.0A, $T_j=25^{\circ}C$		-	2.0	-	V
Short Circuit Current Limit	I_{SC}	1	$T_j=25^{\circ}C$		-	1.1	-	A
Average Temperature Coefficient of Output Voltage	T_{CVO}	1	I_{OUT}=5mA, $0^{\circ}C \leq T_j \leq 125^{\circ}C$		-	-1.0	-	mV/deg

TA78005AP ~ TA78024AP

TA78009AP

ELECTRICAL CHARACTERISTICS (V_{IN}=15V, I_{OUT}=500mA, 0°C≦Tj≦125°C)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Output Voltage	V_{OUT}	1	T_j=25°C, I_{OUT}=100mA		8.64	9.0	9.36	V
Input Regulation	Reg.line	1	Tj=25°C	11.5V≦V_{IN}≦26V	-	7.0	180	mV
				13V≦V_{IN}≦19V	-	2.5	90	
Load Regulation	Reg.load	1	Tj=25°C	5mA≦I_{OUT}≦1.4A	-	12	180	mV
				250mA≦I_{OUT}≦750mA	-	4.0	90	
Output Voltage	V_{OUT}	1	11.5V≦V_{IN}≦2.6V 5.0mA≦I_{OUT}≦1.0A, Po≦15W		8.55	-	9.45	V
Quiescent Current	I_B	1	T_j=25°C, I_{OUT}=5mA		-	4.3	8.0	mA
Quiescent Current Change	ΔI_B	1	11.5V≦V_{IN}≦26V		-	-	1.0	mA
Output Noise Voltage	V_{NO}	1	Ta=25°C, 10Hz≦f≦100kHz IOUT=50mA		-	75	-	μV
Ripple Rejection	RR	1	f=120Hz, 12.5V≦V_{IN}≦22.5V IOUT=50mA, Tj=25°C		56	72	-	dB
Dropout Voltage	V_D	1	I_{OUT}=1.0A, Tj=25°C		-	2.0	-	V
Short Circuit Current Limit	I_{SC}	1	Tj=25°C		-	1.0	-	A
Average Temperature Coefficient of Output Voltage	T_{CVO}	1	I_{OUT}=5mA, 0°C≦Tj≦125°C		-	-1.1	-	mV/deg

TA78010AP

ELECTRICAL CHARACTERISTICS (V_{IN}=16V, I_{OUT}=500mA, 0°C≦T_j≦125°C)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Output Voltage	V_{OUT}	1	T_j=25°C, I_{OTU}=100mA		9.6	10.0	10.4	V
Input Regulation	Reg.line	1	T_j=25°C	12.5V≦V_{IN}≦27V	-	8	200	mV
				14V≦V_{IN}≦20V	-	2.5	100	
Load Regulation	Reg.load	1	T_j=25°C	5mA≦IOUT≦1.4A	-	12	200	mV
				250mA≦I_{OUT}≦750mA	-	4	100	
Output Voltage	V_{OUT}	1	12.5V≦V_{IN}≦25V 5.0mA≦I_{OUT}≦1.0A, P_o≦15W		9.5	-	10.5	V
Quiescent Current	I_B	1	T_j=25°C, I_{OUT}=5mA		-	4.3	8.0	mA
Quiescent Current Change	ΔI_B	1	12.5V≦V_{IN}≦27V		-	-	1.0	mA
Output Noise Voltage	V_{NO}	1	Ta=25°C, 10Hz≦f≦100kHz I_{OUT}=50mA		-	8.0	-	μV
Ripple Rejection	RR	1	f=120Hz, 13.5V≦V_{IN}≦23.5V IOUT=50mA, Tj=25°C		5.5	72	-	dB
Dropout Voltage	V_D	1	IOUT=1.0A, Tj=25°C		-	2.0	-	V
Short Circuit Current	I_{SC}	1	T_j=25°C		-	0.9	-	A
Average Temperature Coefficient of Output Voltage	T_{CVO}	1	I_{OUT}=5mA, 0°C≦T_j≦125°C		-	-1.3	-	mV/deg

TA78005AP～TA78024AP

TA78012AP

ELECTRICAL CHARACTERISTICS (V_{IN}=19V, I_{OUT}=500mA, 0°C≦T_j≦125°C)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Output Voltage	V_{OUT}	1	T_j=25°C, I_{OUT}=100mA		11.5	12.0	12.5	V
Input Regulation	Reg.line	1	T_j=25°C	14.5V≦V_{IN}≦30V	-	10	240	mV
				16V≦V_{IN}≦22V	-	3	120	
Load Regulation	Reg.load	1	T_j=25°C	5mA≦I_{OUT}≦1.4A	-	12	240	mV
				250mA≦I_{OUT}≦750mA	-	4	120	
Output Voltage	V_{OUT}	1	14.5V≦V_{IN}≦27V 5.0mA≦I_{OUT}≦1.0A, P_O≦15W		11.4	-	12.6	V
Quiescent Current	I_B	1	T_j=25°C, I_{OUT}=5mA		-	4.3	8.0	mA
Quiescent Current Change	ΔI_B	1	14.5V≦V_{IN}≦30V		-	-	1.0	mA
Output Noise Voltage	V_{NO}	1	Ta=25°C, 10Hz≦f≦100kHz I_{OUT}=50mA		-	90	-	μV
Repple Rejection	RR	1	f=120Hz, 15V≦V_{IN}≦25V I_{OUT}=50mA, T_j=25°C		55	71	-	dB
Dropout Voltage	V_D	1	I_{OUT}=1.0A, T_j=25°C		-	2.0	-	V
Short Circuit Current	I_{SC}	1	T_j=25°C		-	0.7	-	A
Average Temperature Coefficient of Output Voltage	T_{CVO}	1	I_{OUT}=5mA, 0°C≦T_j≦125°C		-	-1.6	-	mV/deg

TA78005AP ~ TA78024AP

TA78015AP

ELECTRICAL CHARACTERISTICS (V_{IN}=23V, I_{OUT}=500mA, 0°C≦T_j≦125°C)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Output Voltage	V_{OUT}	1	T_j=25°C, I_{OUT}=100mA		14.4	15.0	15.6	V
Input Regulation	Reg.line	1	T_j=25°C	17.5V≦V_{IN}≦30V	-	11	300	mV
				20V≦V_{IN}≦26V	-	3	150	
Load Regulation	Reg.load	1	T_j=25°C	5mA≦I_{OUT}≦1.4A	-	12	300	mV
				250mA≧I_{OUT}≧750mA	-	4	150	
Output Voltage	V_{OUT}	1	17.5V≦V_{IN}≦30V 5.0mA≧I_{OUT}≧1.0A, P_O≧15W		14.25	-	15.75	V
Quiescent Current	I_B	1	T_j=25°C, I_{OUT}=5mA		-	4.4	8.0	mA
Quiescent Current Change	ΔI_B	1	17.5V≦V_{IN}≦30V		-	-	1.0	mA
Output Noise Voltage	V_{NO}	1	Ta=25°C, 10Hz≦f≧100kHz I_{OUT}=50mA		-	110	-	μV
Repple Rejection	RR	1	f=120Hz, 18.5V≦V_{IN}≦28.5V I_{OUT}=50mA, T_j=25°C		54	70	-	dB
Dropout Voltage	V_D	1	I_{OUT}=1.0A, T_j=25°C		-	2.0	-	V
Short Circuit Current	I_{SC}	1	T_j=25°C		-	0.5	-	A
Average Temperature Coefficient of Output Voltage	T_{CVO}	1	I_{OUT}=5mA, 0°C≦T_j≧125°C		-	-2.0	-	mV/deg

TA78005AP ~ TA78024AP

TA78018AP

ELECTRICAL CHARACTERISTICS (V_{IN}=27V, I_{OUT}=500mA, $0^{\circ}C \leq T_j \leq 125^{\circ}C$)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Output Voltage	V_{OUT}	1	$T_j=25^{\circ}C$, I_{OUT}=100mA		17.3	18.0	18.7	V
Input Regulation	Reg·line	1	$T_j=25^{\circ}C$	$21V \leq V_{IN} \leq 33V$	-	13	360	mV
				$24V \leq V_{IN} \leq 30V$	-	4	180	
Load Regulation	Reg·load	1	$T_j=25^{\circ}C$	$5mA \leq I_{OUT} \leq 1.4A$	-	12	360	mV
				$250mA \leq I_{OUT} \leq 750mA$	-	4	180	
Output Voltage	V_{OUT}	1	$21V \leq V_{IN} \leq 33V$ $5.0mA \leq I_{OUT} \leq 1.0A$, $P_O \leq 15W$		17.1	-	18.9	V
Quiescent Current	I_B	1	$T_j=25^{\circ}C$, I_{OUT}=5mA		-	4.5	8.0	mA
Quiescent Current Change	ΔI_B	1	$21V \leq V_{IN} \leq 33V$		-	-	1.0	mA
Output Noise Voltage	V_{NO}	1	$Ta=25^{\circ}C$, $10Hz \leq f \leq 100kHz$ I_{OUT}=50mA		-	125	-	μV
Ripple Rejection	RR	1	f=120Hz, $22V \leq V_{IN} \leq 32V$ I_{OUT}=50mA, $T_j=25^{\circ}C$		52	68	-	dB
Dropout Voltage	V_D	1	I_{OUT}=1.0A, $T_j=25^{\circ}C$		-	2.0	-	V
Short Circuit Current Limit	I_{SC}	1	$T_j=25^{\circ}C$		-	0.4	-	A
Average Temperature Coefficient of Output Voltage	T_{CVO}	1	I_{OUT}=5mA, $0^{\circ}C \leq T_j \leq 125^{\circ}C$		-	-2.5	-	mV/deg

TA78005AP~TA78024AP

TA78020AP

ELECTRICAL CHARACTERISTICS (V_{IN}=29V, I_{OUT}=500mA, $0^{\circ}C \leq T_j \leq 125^{\circ}C$)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Output Voltage	V_{OUT}	1	$T_j=25^{\circ}C$, I_{OUT}=100mA		19.2	20.0	20.8	V
Input Regulation	Reg·line	1	$T_j=25^{\circ}C$	$23V \leq V_{IN} \leq 35V$	-	15	400	mV
				$26V \leq V_{IN} \leq 32V$	-	5	200	
Load Regulation	Reg·load	1	$T_j=25^{\circ}C$	$5mA \leq I_{OUT} \leq 1.4A$	-	12	400	mV
				$250mA \leq I_{OUT} \leq 750mA$	-	4	200	
Output Voltage	V_{OUT}	1	$23V \leq V_{IN} \leq 35V$ $5.0mA \leq I_{OUT} \leq 1.0A$, $P_O \leq 15W$		19.0	-	21.0	V
Quiescent Current	I_B	1	$T_j=25^{\circ}C$, I_{OUT}=5mA		-	4.6	8.0	mA
Quiescent Current Change	ΔI_B	1	$23V \leq V_{IN} \leq 35V$		-	-	1.0	mA
Output Noise Voltage	V_{NO}	1	$Ta=25^{\circ}C$, $10Hz \leq f \leq 100kHz$ I_{OUT}=50mA		-	135	-	μA
Ripple Rejection	RR	1	f=120Hz, $24V \leq V_{IN} \leq 34V$ I_{OUT}=50mA, $T_j=25^{\circ}C$		50	66	-	dB
Dropout Voltage	V_D	1	I_{OUT}=1.0A, $T_j=25^{\circ}C$		-	2.0	-	V
Short Circuit Current Limit	I_{SC}	1	$T_j=25^{\circ}C$		-	0.4	-	A
Average Temperature Coefficient of Output Voltage	T_{CVO}	1	I_{OUT}=5mA, $0^{\circ}C \leq T_j \leq 125^{\circ}C$		-	-3.0	-	mV/deg

TA78005AP～TA78024AP

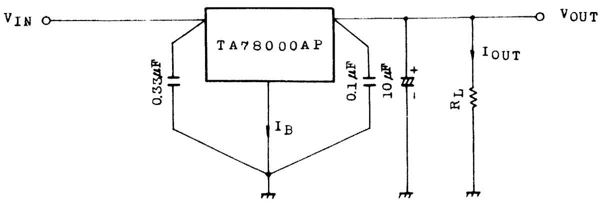
TA78024AP

ELECTRICAL CHARACTERISTICS (V_{IN}=33V, I_{OUT}=500mA, 0°C ≦ T_j ≦ 125°C)

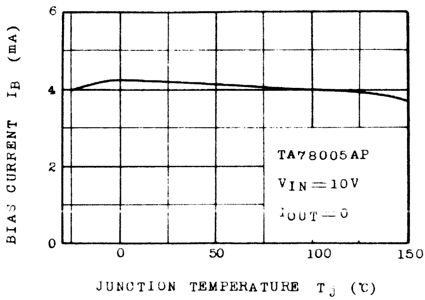
CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Output Voltage	V_{OUT}	1	T_j=25°C, I_{OUT}=100mA		23.0	24.0	25.0	V
Input Regulation	Reg.line	1	T_j=25°C	27V ≦ V_{IN} ≦ 38V	-	18	480	mV
				30V ≦ V_{IN} ≦ 36V	-	6	240	
Load Regulation	Reg.load	1	T_j=25°C	5mA ≦ I_{OUT} ≦ 1.4A	-	12	480	mV
				250mA ≦ I_{OUT} ≦ 750mA	-	4	240	
Output Voltage	V_{OUT}	1	27V ≦ V_{IN} ≦ 38V 5.0mA ≦ I_{OUT} ≦ 1.0A, P_O ≦ 15W		22.8	-	25.2	V
Quiescent Current	I_B	1	T_j=25°C, I_{OUT}=5mA		-	4.6	8.0	mA
Quiescent Current Change	ΔI_B	1	27V ≦ V_{IN} ≦ 38V		-	-	1.0	mA
Output Noise Voltage	V_{NO}	1	Ta=25°C, 10Hz ≦ f ≦ 100kHz I_{OUT}=50mA		-	150	-	μV
Repple Rejection	RR	1	f=120Hz, 28V ≦ V_{IN} ≦ 38V I_{OUT}=50mA, Tj=25°C		50	66	-	dB
Dropout Voltage	V_D	1	I_{OUT}=1.0A, T_j=25°C		-	2.0	-	V
Short Circuit Current	I_{SC}	1	T_j=25°C		-	0.3	-	A
Average Temperature Coefficient of Output Voltage	T_{CVO}	1	I_{OUT}=5mA, 0°C ≦ T_j ≦ 125°C		-	-3.5	-	mV/deg

TA78005AP~TA78024AP

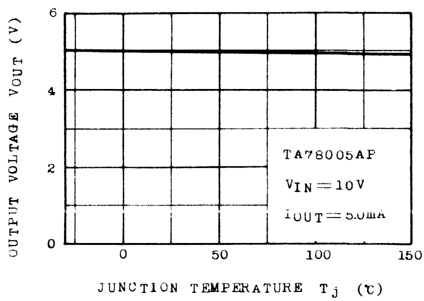
TEST CIRCUIT/STANDARD APPLICATION CIRCUIT



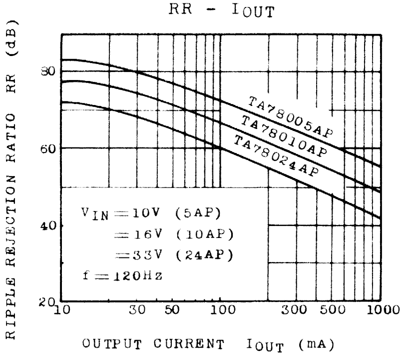
IB - Tj



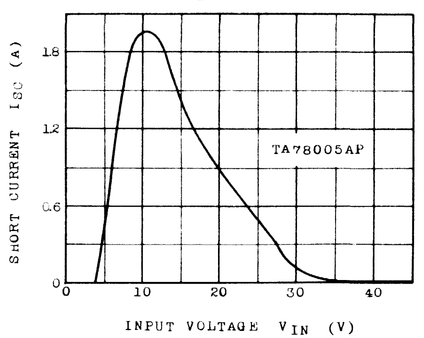
VOUT - Tj



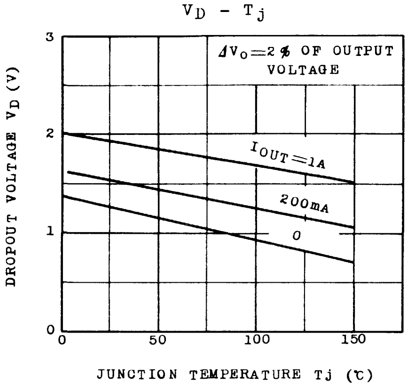
RR - IOUT

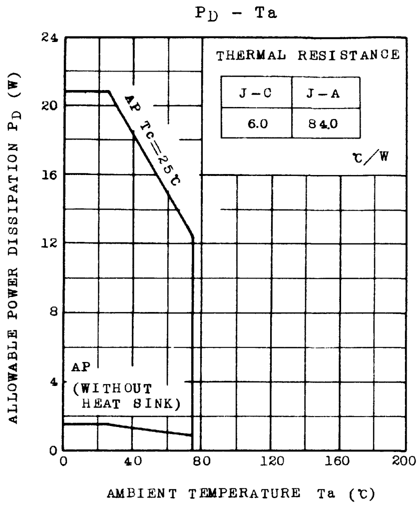


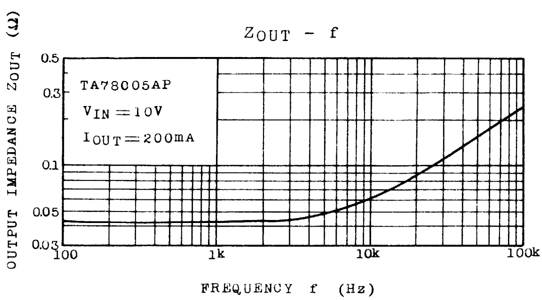
VIN - ISC



TA78005AP～TA78024AP



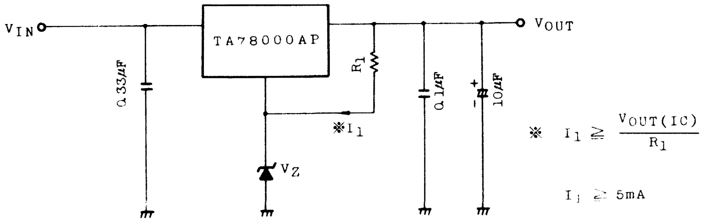




APPLICATION CIRCUITS

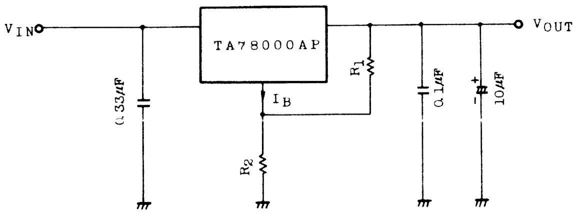
(1) VOLTAGE BOOST REGULATOR

(a) Voltage boost by use of zener diode



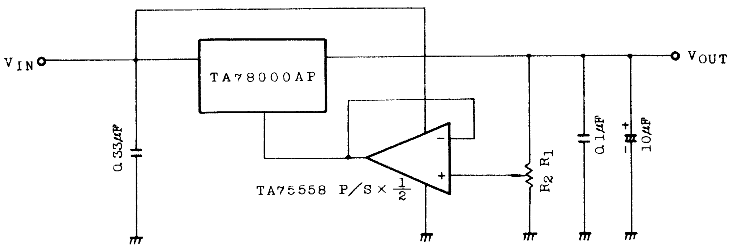
$V_{OUT} = V_{OUT(IC)} + V_Z$

(b) Voltage boost by use of resistor



$V_{OUT} = V_{OUT(IC)} \left(1 + \frac{R_2}{R_1}\right) + R_2 \cdot I_B$

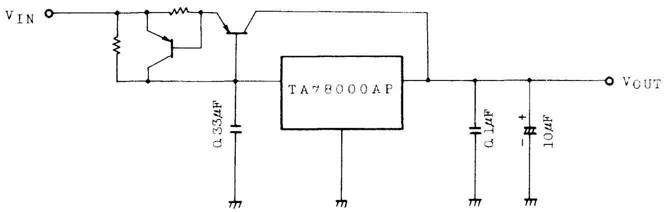
(c) Adjustable output regulator



$V_{OUT} = V_{OUT(IC)} \left(1 + \frac{R_2}{R_1}\right)$

TA78005AP ~ TA78024AP

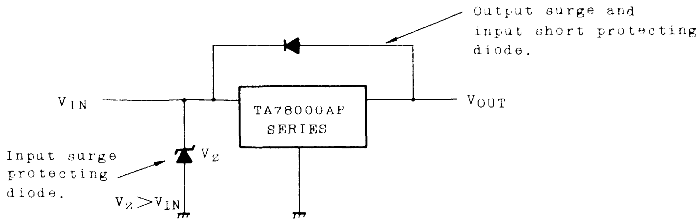
(2) CURRENT BOOST REGULATOR



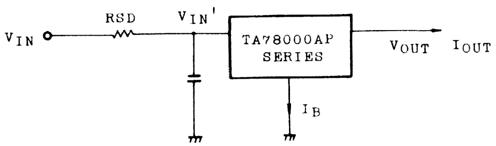
PRECAUTIONS ON APPLICATION

(1) In regard to GND, be careful not to apply a negative voltage to the input/output terminal. Further, special care is necessary in case of a voltage boost application.

(2) When a surge voltage exceeding maximum rating is applied to the input terminal or when a voltage in excess of the input terminal voltage is applied to the output terminal, the circuit may be destroyed.
Specially, in the latter case, great care is necessary
Further, if the input terminal shorts to GND in a state of normal operation, the output terminal voltage becomes higher than the input voltage (GND potential), and the electric charge of a chemical capacitor connected to the output terminal flows into the input side, which may cause the destruction of circuit.
In these cases, take such steps as a zener diode and a general silicon diode are connected to the circuit, as shown in the following figure.



(3) When the input voltage is too high, the power dissipation of three terminal regulator increases because of series regulator, so that the junction temperature rises. In such a case, it is recommended to reduce the power dissipation by inserting the power limiting resistor RSD in the input terminal, and to reduce the junction temperature as a result.



The power dissipation P_D of IC is expressed in the following equation.

$$P_D = (V_{IN}'-V_{OUT}) \cdot I_{OUT} + V_{IN}' \cdot I_B$$

If V_{IN}' is reduced below the lowest voltage necessary for the IC, the parasitic oscillation will be caused according to circumstances.
In determing the resistance value of R_{SD}, design with margin should be made by making reference to the following equation.

$$R_{SD} < \frac{V_{IN} - V_{IN}'}{I_{OUT} + I_B}$$

(4) Connect the input terminal and GND, and the output terminal and GND, by capacitor respectively. The capacitances should be determind experimentally because they depend on prented patterns. In particular, adequate investigation should be made so that there is no problem even at time of high or low temperature.

(5) Installation of IC for power supply
For obtaining high reliability on the heat sink design of the regulator IC, it is generally required to derate more than 20% of maximum junction temperature (Tj MAX.).
Further, full consideration should be given to the installation of IC to the heat sink.

TA78005AP~TA78024AP

(a) Heat sink design

The thermal resistance of IC itself is required from the viewpoint of the design of elements, but the thermal resistance from the IC package to the open air varies with the contact thermal resistance.
Table 1 shows how much the value of the contact thermal resistance ($Q_c + Q_s$) is changed by insulating sheet (mica) and heat sink grease.

TABLE

Unit: °C/W

PACKAGE	MODEL No.	TORQUE	MICA	$Q_c + Q_s$
TO-220AB	TA780×××AP	6kg.cm	Not Provided	0.3∿0.5(1.5∿2.0)
			Provided	2.0∿2.5(4.0∿6.0)

The figures given in parentheses denote the values at time of no grease.

The package of regulator IC serves as GND, therefore, usually use the value at time of "no mica."

(b) Silicon grease

When a circuit not exceeding maximum rating is designed, it is to be desired that the grease should be used if possible. If it is required that the contact thermal resistance is reduced from the viewpoint of the circuit design, it is recommended that the following methods be adopted.

A: Use Thercon (Fuji High Polymer Kogyo K.K.)

B: Use SC101 (Torei Silicon) or G-640 (GE), if grease is used.

(c) Torque

When installing IC on a heat sink or the like, tighten the IC with the torque of less than the rated value. If it is tightened with the torque in excess of the rated value, sometimes the internal elements of the IC are adversely affected. Therefore, great care should be given to the installing operation.
Further, if polycarbonate screws are used, the torque causes a change with the passage of time, which may lessen the effect of radiation.

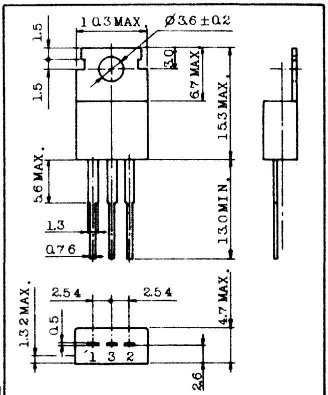
BIPOLAR LINEAR INTEGRATED CIRCUIT
SILICON MONOLITHIC

TA78M05P~TA78M24P

0.5A THREE TERMINAL POSITIVE VOLTAGE REGULATORS
5V, 6V, 8V, 9V, 10V, 12V, 15V, 18V, 20V, 24V

- Suitable for C-MOS, TTL, and the other Digital IC Power Supply.
- Output Current in Excess of 0.5A
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Packaged in the Plastic Case TO-220AB

Unit in mm



1. INPUT
2. OUTPUT
3. GND (CASE)

JEDEC	TO−220AB
EIAJ	SC−46
TOSHIBA	5−10A

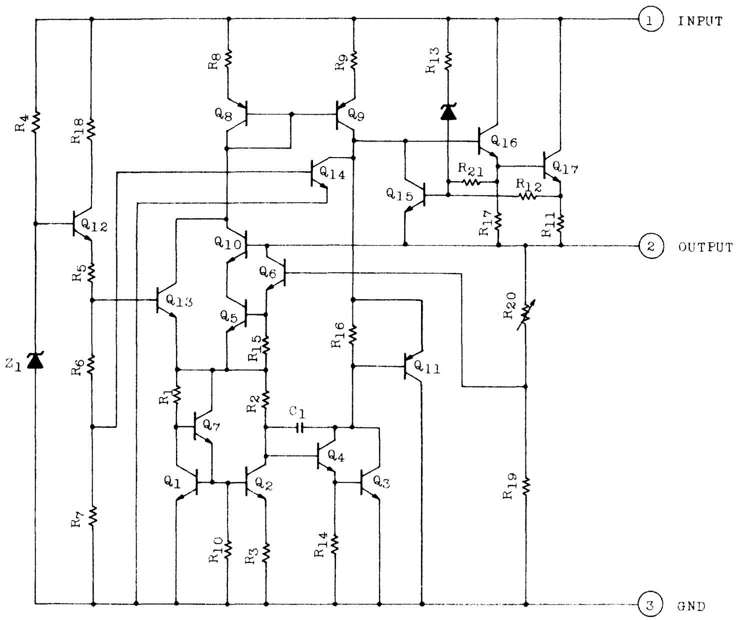
Mounting Kit No. AC75

MAXIMUM RATINGS (Ta=25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Input Voltage	TA78M05P	V_{IN}	35	V
	TA78M06P			
	TA78M08P			
	TA78M09P			
	TA78M10P			
	TA78M12P			
	TA78M15P			
Input Voltage	TA78M18P	V_{IN}	40	V
	TA78M20P			
	TA78M24P			
Power Dissipation (Tc=25°C)		P_D	20.8	W
Operating Temperature		Topr	-30~75	°C
Storage Temperature		Tstg	-55~150	°C

TA78M05P～TA78M24P

EQUIVALENT CIRCUIT



TA78M05P ~ TA78M24P

TA78M05P

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{IN}=10V, I_{OUT}=350mA, 0°C ≦ Tj ≦ 125°C
C_{IN}=0.33μF, C_{OUT}=0.1μF

CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Output Voltage		V_{OUT}	1	Tj=25°C		4.8	5.0	5.2	V
Input Regulation		Reg·Line	1	Tj=25°C	7V ≦ V_{IN} ≦ 25V, I_{OUT}=200mA	-	4	100	mV
					8V ≦ V_{IN} ≦ 25V, I_{OUT}=200mA	-	2	50	mV
Load Regulation		Reg·Load	1	Tj=25°C	5mA ≦ I_{OUT} ≦ 500mA	-	25	100	mV
					5mA ≦ I_{OUT} ≦ 200mA	-	10	50	mV
Output Voltage		V_{OUT}	1	7V ≦ V_{IN} ≦ 20V, 5mA ≦ I_{OUT} ≦ 350mA		4.75	-	5.25	V
Quiescent Current		I_B	1	Tj=25°C		-	4.7	6.0	mA
Quiescent Current Charge	Line	ΔI_{BO}	1	8.5V ≦ V_{IN} ≦ 25.5V, I_{OUT}=200mA		-	-	0.8	mA
	Load	ΔI_{BI}	1	5mA ≦ I_{OUT} ≦ 350mA		-	-	0.5	mA
Output Noise Voltage		V_{NO}	2	Ta=25°C, 10Hz ≦ f ≦ 100kHz		-	50	200	μV
Ripple Rejection		RR	3	f=120Hz, I_{OUT}=100mA, 8V ≦ V_{IN} ≦ 18V		62	69	-	dB
Short Circuit Current Limit		I_{SC}	1	Tj=25°C		-	960	-	mA
Average Temperature Coefficient Output Voltage		T_{CVO}	1	I_{OUT}=5mA		-	-0.7	-	mV/deg
Dropout Voltage		V_D	1	Ta=25°C		-	1.7	-	V

TA78M05P～TA78M24P

TA78M06P

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{IN}=11V, I_{OUT}=350mA, 0°C≦Tj≦125°C
C_{IN}=0.33μF, C_{OUT}=0.1μF

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Output Voltage		V_{OUT}	1	Tj=25°C		5.75	6.0	6.25	V
Input Regulation		Reg·Line	1	Tj=25°C	8V≦V_{IN}≦25V I_{OUT}=200mA	-	4	100	mV
					9V≦V_{IN}≦25V I_{OUT}=200mA	-	2	50	mV
Load Regulation		Reg·Load	1	Tj=25°C	5mA≦I_{OUT}≦500mA	-	25	120	mV
					5mA≦I_{OUT}≦200mA	-	10	60	mV
Output Voltage		V_{OUT}	1	8V≦V_{IN}≦21V 5mA≦I_{OUT}≦350mA		5.7	-	6.3	V
Quiescent Current		I_B	1	Tj=25°C		-	4.7	6.0	mA
Quiescent Current Charge	Line	ΔI_{BO}	1	9.5V≦V_{IN}≦25.5V I_{OUT}=200mA		-	-	0.8	mA
	Load	ΔI_{BI}	1	5mA≦I_{OUT}≦350mA		-	-	0.5	mA
Output Noise Voltage		V_{NO}	2	Ta=25°C, 10Hz≦f≦100kHz		-	55	220	μV
Ripple Rejection		RR	3	f=120Hz, I_{OUT}=100mA 9V≦V_{IN}≦19V		59	66	-	dB
Short Circuit Current Limit		I_{SC}	1	Tj=25°C		-	960	-	mA
Average Temperature Coefficient Output Voltage		T_{CVO}	1	I_{OUT}=5mA		-	-0.8	-	mV/deg
Dropout Voltage		V_D	1	Ta=25°C		-	1.7	-	V

TA78M08P

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{IN}=14V, I_{OUT}=350mA, 0°C≤Tj≤125°C
C_{IN}=0.33μF, C_{OUT}=0.1μF

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Output Voltage		V_{OUT}	1	Tj=25°C		7.7	8.0	8.3	V
Input Regulation		Reg·Line	1	Tj=25°C	10.5V≤V_{IN}≤25V I_{OUT}=200mA	–	5	100	mV
					11V≤V_{IN}≤25V I_{OUT}=200mA	–	3	50	mV
Load Regulation		Reg·Load	1	Tj=25°C	5mA≤I_{OUT}≤500mA	–	26	160	mV
					5mA≤I_{OUT}≤200mA	–	10	80	mV
Output Voltage		V_{OUT}	1	10.5V≤V_{IN}≤23V 5mA≤I_{OUT}≤350mA		7.6	–	8.4	V
Quiescent Current		I_B	1	Tj=25°C		–	4.7	6.0	mA
Quiescent Current Charge	Line	ΔI_{BO}	1	11V≤V_{IN}≤25.5V I_{OUT}=200mA		–	–	0.8	mA
	Load	ΔI_{BI}	1	5mA≤I_{OUT}≤350mA		–	–	0.5	mA
Output Noise Voltage		V_{NO}	2	Ta=25°C, 10Hz≤f≤100kHz		–	60	250	μV
Ripple Rejection		RR	3	f=120Hz, I_{OUT}=100mA 11.5V≤V_{IN}≤21.5V		56	63	–	dB
Short Circuit Current Limit		I_{SC}	1	Tj=25°C		–	960	–	mA
Average Temperature Coefficient Output Voltage		T_{CVO}	1	I_{OUT}=5mA		–	-1.1	–	mV/deg
Dropout Voltage		V_D	1	Ta=25°C		–	1.7	–	V

TA78M05P~TA78M24P

TA78M09P

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{IN}=15V, I_{OUT}=350mA, 0°C≦Tj≦125°C

C_{IN}=0.33μF, C_{OUT}=0.1μF

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Output Voltage		V_{OUT}	1	Tj=25°C		8.64	9.0	9.36	V
Input Regulation		Reg·Line	1	Tj=25°C	11.5V≦V_{IN}≦26V I_{OUT}=200mA	-	5	100	mV
					13V≦V_{IN}≦26V I_{OUT}=200mA	-	3	50	mV
Load Regulation		Reg·Load	1	Tj=25°C	5mA≦I_{OUT}≦500mA	-	26	180	mV
					5mA≦I_{OUT}≦200mA	-	10	90	mV
Output Voltage		V_{OUT}	1	11.5V≦V_{IN}≦24V 5mA≦I_{OUT}≦350mA		8.55	-	9.45	V
Quiescent Current		I_B	1	Tj=25°C		-	4.7	6.0	mA
Quiescent Current Charge	Line	ΔI_{BO}	1	12V≦V_{IN}≦26.5V I_{OUT}=200mA		-	-	0.8	mA
	Load	ΔI_{BI}	1	5mA≦I_{OUT}≦350mA		-	-	0.5	mA
Output Noise Voltage		V_{NO}	2	Ta=25°C, 10Hz≦f≦100kHz		-	60	270	μV
Ripple Rejection		RR	3	f=120Hz, I_{OUT}=100mA 12.5V≦V_{IN}≦22.5V		56	63	-	dB
Short Circuit Current Limit		I_{SC}	1	Tj=25°C		-	960	-	mA
Average Temperature Coefficient Output Voltage		T_{CVO}	1	I_{OUT}=5mA		-	-1.3	-	mV/deg
Dropout Voltage		V_D	1	Ta=25°C		-	1.7	-	V

TA78M10P

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{IN}=16V, I_{OUT}=350mA, 0°C≦Tj≦125°C
C_{IN}=0.33μF, C_{OUT}=0.1μF

CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Output Voltage		V_{OUT}	1	Tj=25°C		9.6	10.0	10.4	V
Input Regulation		Reg·Line	1	Tj=25°C	12.5V≦V_{IN}≦26V, I_{OUT}=200mA	-	6	100	mV
					14V≦V_{IN}≦26V, I_{OUT}=200mA	-	3	50	mV
Load Regulation		Reg·Load	1	Tj=25°C	5mA≦I_{OUT}≦500mA	-	26	200	mV
					5mA≦I_{OUT}≦200mA	-	10	100	mV
Output Voltage		V_{OUT}	1	12.5V≦V_{IN}≦25V, 5mA≦I_{OUT}≦350mA		9.5	-	10.5	V
Quiescent Current		I_B	1	Tj=25°C		-	4.7	6.0	mA
Quiescent Current Charge	Line	ΔI_{BO}	1	13V≦V_{IN}≦26.5V, I_{OUT}=200mA		-	-	0.8	mA
	Load	ΔI_{BI}	1	5mA≦I_{OUT}≦350mA		-	-	0.5	mA
Output Noise Voltage		V_{NO}	2	Ta=25°C, 10Hz≦f≦100kHz		-	65	280	μV
Ripple Rejection		RR	3	f=120Hz, I_{OUT}=100mA, 13.5V≦V_{IN}≦23.5V		55	62	-	dB
Short Circuit Current Limit		I_{SC}	1	Tj=25°C		-	960	-	mA
Average Temperature Coefficient Output Voltage		T_{CVO}	1	I_{OUT}=5mA		-	-1.4	-	mV/deg
Dropout Voltage		V_D	1	Ta=25°C		-	1.7	-	V

TA78M05P～TA78M24P

TA78M12P

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{IN}=19V, I_{OUT}=350mA, 0°C≦Tj≦125°C
C_{IN}=0.33μF, C_{OUT}=0.1μF

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Output Voltage		V_{OUT}	1	Tj=25°C		11.5	12.0	12.5	V
Input Regulation		Reg·Line	1	Tj=25°C	14.5V≦V_{IN}≦30V I_{OUT}=200mA	–	7	100	mV
					16V≦V_{IN}≦30V I_{OUT}=200mA	–	3	50	mV
Load Regulation		Reg·Load	1	Tj=25°C	5mA≦I_{OUT}≦500mA	–	27	240	mV
					5mA≦I_{OUT}≦200mA	–	10	120	mV
Output Voltage		V_{OUT}	1	14.5V≦V_{IN}≦27V 5mA≦I_{OUT}≦350mA		11.4	–	12.6	V
Quiescent Current		I_B	1	Tj=25°C		–	4.7	6.0	mA
Quiescent Current Charge	Line	ΔI_{BO}	1	15V≦V_{IN}≦30.5V I_{OUT}=200mA		–	–	0.8	mA
	Load	ΔI_{BI}	1	5mA≦I_{OUT}≦350mA		–	–	0.5	mA
Output Noise Voltage		V_{NO}	2	Ta=25°C, 10Hz≦f≦100kHz		–	70	300	μV
Ripple Rejection		RR	3	f=120Hz, I_{OUT}=100mA 15V≦V_{IN}≦35V		55	62	–	dB
Short Circuit Current Limit		I_{SC}	1	Tj=25°C		–	960	–	mA
Average Temperature Coefficient Output Voltage		T_{CVO}	1	I_{OUT}=5mA		–	-1.7	–	mV/deg
Dropout Voltage		V_D	1	Ta=25°C		–	1.7	–	V

TA78M15P

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{IN}=23V, I_{OUT}=350mA, 0°C≦Tj≦125°C
C_{IN}=0.33μF, C_{OUT}=0.1μF

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Output Voltage		V_{OUT}	1	Tj=25°C		14.4	15.0	15.6	V
Input Regulation		Reg·Line	1	Tj=25°C	17.5V≦V_{IN}≦30V, I_{OUT}=200mA	–	8	100	mV
					20V≦V_{IN}≦30V, I_{OUT}=200mA	–	4	50	mV
Load Regulation		Reg·Load	1	Tj=25°C	5mA≦I_{OUT}≦500mA	–	27	300	mV
					5mA≦I_{OUT}≦200mA	–	10	150	mV
Output Voltage		V_{OUT}	1	17.5V≦V_{IN}≦30V, 5mA≦I_{OUT}≦350mA		14.25	–	15.75	V
Quiescent Current		I_B	1	Tj=25°C		–	4.7	6.0	mA
Quiescent Current Charge	Line	ΔI_{BO}	1	18V≦V_{IN}≦30.5V, I_{OUT}=200mA		–	–	0.8	mA
	Load	ΔI_{BI}	1	5mA≦I_{OUT}≦350mA		–	–	0.5	mA
Output Noise Voltage		V_{NO}	2	Ta=25°C, 10Hz≦f≦100kHz		–	80	450	μV
Ripple Rejection		RR	3	f=120Hz, I_{OUT}=100mA, 18.5V≦V_{IN}≦28.5V		54	61	–	dB
Short Circuit Current Limit		I_{SC}	1	Tj=25°C		–	960	–	mA
Average Temperature Coefficient Output Voltage		T_{CVO}	1	I_{OUT}=5mA		–	-2.1	–	mV/deg
Dropout Voltage		V_D	1	Ta=25°C		–	1.7	–	V

TA78M05P～TA78M24P

TA78M18P

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{IN}=27V, I_{OUT}=350mA, 0°C≦Tj≦125°C
C_{IN}=0.33μF, C_{OUT}=0.1μF

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Output Voltage		V_{OUT}	1	Tj=25°C		17.3	18.0	18.7	V
Input Regulation		Reg·Line	1	Tj=25°C	21V≦V_{IN}≦33V I_{OUT}=200mA	-	9	100	mV
					24V≦V_{IN}≦33V I_{OUT}=200mA	-	5	50	mV
Load Regulation		Reg·Load	1	Tj=25°C	5mA≦I_{OUT}≦500mA	-	28	360	mV
					5mA≦I_{OUT}≦200mA	-	10	180	mV
Output Voltage		V_{OUT}	1	21V≦V_{IN}≦33V 5mA≦I_{OUT}≦350mA		17.1	-	18.9	V
Quiescent Current		I_B	1	Tj=25°C		-	4.7	6.0	mA
Quiescent Current Charge	Line	ΔI_{BO}	1	21.5V≦V_{IN}≦33.5V I_{OUT}=200mA		-	-	0.8	mA
	Load	ΔI_{BI}	1	5mA≦I_{OUT}≦350mA		-	-	0.5	mA
Output Noise Voltage		V_{NO}	2	Ta=25°C, 10Hz≦f≦100kHz		-	90	490	μV
Ripple Rejection		RR	3	f=120Hz, I_{OUT}=100mA 22V≦V_{IN}≦32V		53	60	-	dB
Short Circuit Current Limit		I_{SC}	1	Tj=25°C		-	960	-	mA
Average Temperature Coefficient Output Voltage		T_{CVO}	1	I_{OUT}=5mA		-	-2.6	-	mV/deg
Dropout Voltage		V_D	1	Ta=25°C		-	1.7	-	V

TA78M20P

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{IN}=29V, I_{OUT}=350mA, 0°C≦Tj≦125°C

C_{IN}=0.33μF, C_{OUT}=0.1μF

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Output Voltage		V_{OUT}	1	Tj=25°C		19.2	20.0	20.8	V
Input Regulation		Reg·Line	1	Tj=25°C	23V≦V_{IN}≦35V I_{OUT}=200mA	-	10	100	mV
					24V≦V_{IN}≦35V I_{OUT}=200mA	-	6	50	mV
Load Regulation		Reg·Load	1	Tj=25°C	5mA≦I_{OUT}≦500mA	-	28	400	mV
					5mA≦I_{OUT}≦200mA	-	10	200	mV
Output Voltage		V_{OUT}	1	23V≦V_{IN}≦35V 5mA≦I_{OUT}≦350mA		19.0	-	21.0	V
Quiescent Current		I_B	1	Tj=25°C		-	4.7	6.0	mA
Quiescent Current Charge	Line	ΔI_{BO}	1	23.5V≦V_{IN}≦35.5V I_{OUT}=200mA		-	-	0.8	mA
	Load	ΔI_{BI}	1	5mA≦I_{OUT}≦350mA		-	-	0.5	mA
Output Noise Voltage		V_{NO}	2	Ta=25°C, 10Hz≦f≦100kHz		-	95	540	μV
Ripple Rejection		RR	3	f=120Hz, I_{OUT}=100mA 24V≦V_{IN}≦34V		53	60	-	dB
Short Circuit Current Limit		I_{SC}	1	Tj=25°C		-	960	-	mA
Average Temperature Coefficient Output Voltage		T_{CVO}	1	I_{OUT}=5mA		-	-2.9	-	mV/deg
Dropout Voltage		V_D	1	Ta=25°C		-	1.7	-	V

TA78M05P～TA78M24P

TA78M24P

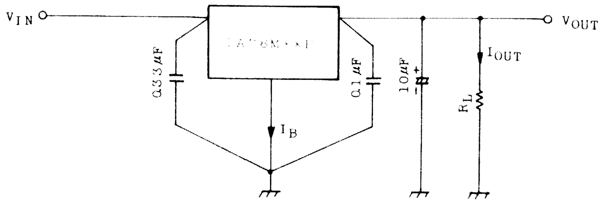
ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{IN}=33V, I_{OUT}=350mA, 0°C≦Tj≦125°C
C_{IN}=0.33μF, C_{OUT}=0.1μF

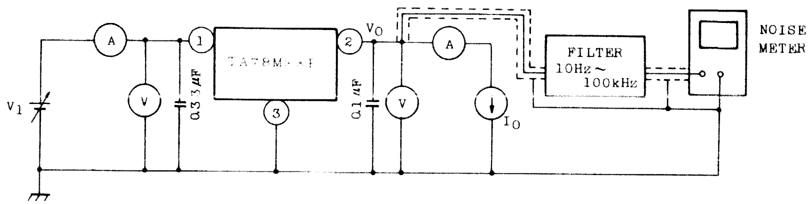
CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Output Voltage		V_{OUT}	1	Tj=25°C		23.0	24.0	25.0	V
Input Regulation		Reg・Line	1	Tj=25°C	27V≦V_{IN}≦38V I_{OUT}=200mA	-	12	100	mV
					28V≦V_{IN}≦38V I_{OUT}=200mA	-	7	50	mV
Load Regulation		Reg・Load	1	Tj=25°C	5mA≦I_{OUT}≦500mA	-	30	480	mV
					5mA≦I_{OUT}≦200mA	-	10	240	mV
Output Voltage		V_{OUT}	1	27V≦V_{IN}≦38V 5mA≦I_{OUT}≦350mA		22.8	-	25.2	V
Quiescent Current		I_B	1	Tj=25°C		-	4.7	6.0	mA
Quiescent Current Charge	Line	ΔI_{BO}	1	27.5V≦V_{IN}≦38.5V I_{OUT}=200mA		-	-	0.8	mA
	Load	ΔI_{BI}	1	5mA≦I_{OUT}≦350mA		-	-	0.5	mA
Output Noise Voltage		V_{NO}	2	Ta=25°C, 10Hz≦f≦100kHz		-	115	650	μV
Ripple Rejection		RR	3	f=120Hz, I_{OUT}=100mA 28V≦V_{IN}≦38V		50	57	-	dB
Short Circuit Current Limit		I_{SC}	1	Tj=25°C		-	960	-	mA
Average Temperature Coefficient Output Voltage		T_{CVO}	1	I_{OUT}=5mA		-	-3.8	-	mV/deg
Dropout Voltage		V_D	1	Ta=25°C		-	1.7	-	V

TA78M05P~TA78M24P

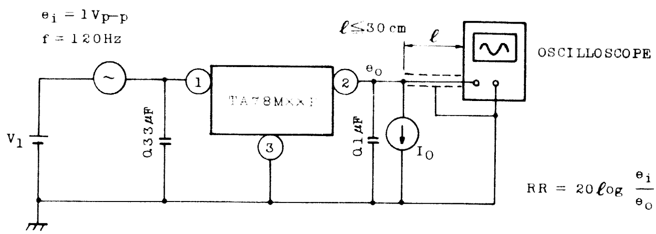
TEST CIRCUIT 1 / STANDARD APPLICATION



TEST CIRCUIT 2 V_{NO}



TEST CIRCUIT 3 R.R.



$$RR = 20 \ell og \frac{e_i}{e_o} \text{ (dB)}$$

TA78L005P/AP ~ TA78L024P/AP

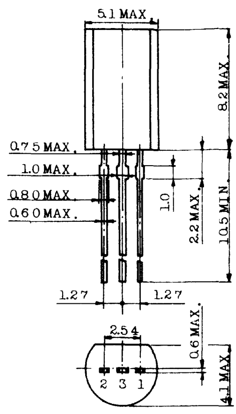
BIPOLAR LINEAR INTEGRATED CIRCUIT
SILICON MONOLITHIC

THREE TERMINAL POSITIVE REGULATORS

5V, 6V, 7V, 7.5V, 8V, 9V, 10V, 12V,
13.2V, 15V, 18V, 20V, 24V.

- Suitable for TTL, DTL, HTL, C-MOS Power Supply
- Internal Short-Circuit Current Limiting
- Internal Thermal Overload Protection
- Maximum Output Current of 150mA ($T_j=25^\circ C$)
- Available in the Plastic TO-92MOD Package

Unit in mm



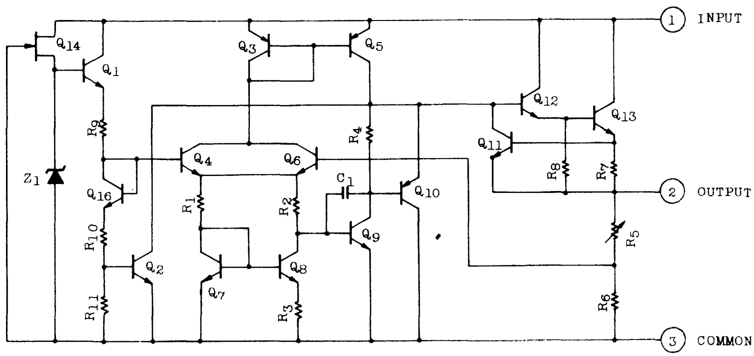
1. INPUT
2. OUTPUT
3. COMMON

JEDEC	TO-92MOD
EIAJ	—
TOSHIBA	5-5

MAXIMUM RATINGS ($Ta=25^\circ C$)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Input Voltage	(5V ~ 15V)	V_{IN}	35	V
	(18V ~ 24V)		40	
Power Dissipation		P_D	800	mW
Operating Temperature		T_{opr}	-30 ~ 75	$^\circ C$
Storage Temperature		T_{stg}	-55 ~ 150	$^\circ C$

EQUIVALENT CIRCUIT



TA78L005P/AP ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, V_{IN}=10V, I_{OUT}=40mA, C_{IN}=0.33μF, C_{OUT}=0.1μF, $0^{o}C < T_j < 125^{o}C$)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION		TA78L005P MIN.	TA78L005P TYP.	TA78L005P MAX.	TA78L005AP MIN.	TA78L005AP TYP.	TA78L005AP MAX.	UNIT
Output Voltage	V_{OUT}	1	$T_j=25^{o}C$		4.68	5.0	5.32	4.8	5.0	5.2	V
Input Regulation	Reg.line	1	$T_j=25^{o}C$	$7.0 \leqq V_{IN} \leqq 20V$	-	55	200	-	55	150	mV
				$8.0 \leqq V_{IN} \leqq 20V$	-	45	150	-	45	100	
Load Regulation	Reg.load	1	$T_j=25^{o}C$	$1.0mA \leqq I_{OUT} \leqq 100mA$	-	11	60	-	11	60	mV
				$1.0mA \leqq I_{OUT} \leqq 40mA$	-	5.0	30	-	5.0	30	
Output Voltage	V_{OUT}	1	$7.0V \leqq V_{IN} \leqq 20V$, $1.0mA \leqq I_{OUT} \leqq 40mA$		4.6	-	5.4	4.75	-	5.25	V
			V_{IN}=10V, $1.0mA \leqq I_{OUT} \leqq 70mA$		4.6	-	5.4	4.75	-	5.25	
Quiescent Current	I_B	1	$T_j=25^{o}C$		-	3.1	6.0	-	3.1	6.0	mA
			$T_j=125^{o}C$		-	-	5.5	-	-	5.5	
Quiescent Current Change	ΔI_B	1	$8.0V \leqq V_{IN} \leqq 20V$		-	-	1.5	-	-	1.5	mA
			$1.0mA \leqq I_{OUT} \leqq 40mA$		-	-	0.2	-	-	0.1	
Output Noise Voltage	V_{NO}	1	$Ta=25^{o}C$, $10Hz \leqq f \leqq 100kHz$		-	40	-	-	40	-	μV
Long Term Stability	$\Delta V_{OUT}/\Delta t$	1			-	12	-	-	12	-	mV/1.0 KHrs
Ripple Rejection	RR	2	f=120Hz, $8.0V \leqq V_{IN} \leqq 18V$, $T_j=25^{o}C$		40	49	-	41	49	-	dB
Dropout Voltage	$\lvert V_{IN}-V_{OUT} \rvert$	1	$T_j=25^{o}C$		-	1.7	-	-	1.7	-	V
Average Temperature Coefficient of Output Voltage	TC_{VO}	1	I_{OUT}=5mA		-	-0.6	-	-	-0.6	-	$mV/^{o}C$

TA78L005P/AP ~ TA78L024P/AP

TA78L006P/AP ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, V_{IN}=11V, I_{OUT}=40mA, C_{IN}=0.33μF, C_{OUT}=0.1μF, $0^{\circ}C < T_j < 125^{\circ}C$)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION		TA78L006P MIN.	TA78L006P TYP.	TA78L006P MAX.	TA78L006AP MIN.	TA78L006AP TYP.	TA78L006AP MAX.	UNIT
Output Voltage	V_{OUT}	1	$T_j=25^{\circ}C$		5.61	6.0	6.39	5.76	6.0	6.24	V
Input Regulation	Reg.line	1	$T_j=25^{\circ}C$	$8.1V \leq V_{IN} \leq 21V$	-	50	200	-	50	150	mV
				$9.0V \leq V_{IN} \leq 21V$	-	45	150	-	45	110	
Load Regulation	Reg.load	1	$T_j=25^{\circ}C$	$1.0mA \leq I_{OUT} \leq 100mA$	-	12	70	-	12	70	mV
				$1.0mA \leq I_{OUT} \leq 40mA$	-	5.5	35	-	5.5	35	
Output Voltage	V_{OUT}	1	$8.1V \leq V_{IN} \leq 21V$, $1.0mA \leq I_{OUT} \leq 40mA$		5.52	-	6.48	5.7	-	6.3	V
			$V_{IN}=11V$, $1.0mA \leq I_{OUT} \leq 70mA$		5.52	-	6.48	5.7	-	6.3	
Quiescent Current	I_B	1	$T_j=25^{\circ}C$		-	3.1	6.0	-	3.1	6.0	mA
			$T_j=125^{\circ}C$		-	-	5.5	-	-	5.5	
Quiescent Current Change	ΔI_B	1	$9.0V \leq V_{IN} \leq 20V$		-	-	1.5	-	-	1.5	mA
			$1.0mA \leq I_{OUT} \leq 40mA$		-	-	0.2	-	-	0.1	
Output Noise Voltage	V_{NO}	1	$Ta=25^{\circ}C$, $10Hz \leq f \leq 100kHz$		-	40	-	-	40	-	μV
Long Term Stability	$\Delta V_{OUT}/\Delta t$	1			-	14	-	-	14	-	mV/1.0 KHrs
Ripple Rejection	RR	2	f=120Hz, $9.0V \leq V_{IN} \leq 19V$, $T_j=25^{\circ}C$		38	47	-	39	47	-	dB
Dropout Voltage	$\lvert V_{IN}-V_{OUT} \rvert$	1	$T_j=25^{\circ}C$		-	1.7	-	-	1.7	-	V
Average Temperature Coefficient of Output Voltage	TC_{VO}	1	I_{OUT}=5mA		-	-0.7	-	-	-0.7	-	mV/°C

TA78L007P/AP ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, V_{IN}=12V, I_{OUT}=40mA, C_{IN}=0.33μF, C_{OUT}=0.1μF, 0°C<T_j<125°C)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION		TA78L007P MIN.	TA78L007P TYP.	TA78L007P MAX.	TA78L007AP MIN.	TA78L007AP TYP.	TA78L007AP MAX.	UNIT
Output Voltage	V_{OUT}	1	T_j=25°C		6.55	7.0	7.45	6.72	7.0	7.28	V
Input Regulation	Reg.line	1	T_j=25°C	9.2V≦V_{IN}≦22V	-	50	200	-	50	160	mV
				10V≦V_{IN}≦22V	-	45	150	-	45	115	
Load Regulation	Reg.load	1	T_j=25°C	1.0mA≦I_{OUT}≦100mA	-	13	75	-	13	75	mV
				1.0mA≦I_{OUT}≦40mA	-	6.0	40	-	6.0	40	
Output Voltage	V_{OUT}	1	9.2V≦V_{IN}≦22V, 1.0mA≦I_{OUT}≦40mA		6.44	-	7.36	6.65	-	7.35	V
			V_{IN}=12V, 1.0mA≦I_{OUT}≦70mA		6.44	-	7.56	6.65	-	7.35	
Quiescent Current	I_B	1	T_j=25°C		-	3.1	6.5	-	3.1	6.5	mA
			T_j=125°C		-	-	6.0	-	-	6.0	
Quiescent Current Change	ΔI_B	1	10V≦V_{IN}≦22V		-	-	1.5	-	-	1.5	mA
			1.0mA≦I_{OUT}≦40mA		-	-	0.2	-	-	0.1	
Output Noise Voltage	V_{NO}	1	Ta=25°C, 10Hz≦f≦100kHz		-	50	-	-	50	-	μV
Long Term Stability	$\Delta V_{OUT}/\Delta t$	1			-	17	-	-	17	-	mV/1.0 KHrs
Ripple Rejection	RR	2	f=120Hz, 10V≦V_{IN}≦20V, T_j=25°C		36	46	-	37	46	-	dB
Dropout Voltage	$\lvert V_{IN}-V_{OUT}\rvert$	1	T_j=25°C		-	1.7	-	-	1.7	-	V
Average Temperature Coefficient of Output Voltage	TC_{VO}	1	I_{OUT}=5mA		-	-0.75	-	-	-0.75	-	mV/°C

TA78L005P/AP ~TA78L024P/AP

TA78L07 P/AP ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, V_{IN}=13V, I_{OUT}=40mA, C_{IN}=0.33μF, C_{OUT}=0.1μF, 0°C <T_j <125°C)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION		TA78L075P MIN.	TA78L075P TYP.	TA78L075P MAX.	TA78L075AP MIN.	TA78L075AP TYP.	TA78L075AP MAX.	UNIT
Output Voltage	V_{OUT}	1	T_j=25°C		7.02	7.5	7.98	7.21	7.5	7.79	V
Input Regulation	Reg.line	1	T_j=25°C	9.8V≦V_{IN}≦23V	-	40	200	-	40	170	mV
				10.5V≦V_{IN}≦23V	-	40	150	-	40	120	
Load Regulation	Reg.load	1	T_j=25°C	1.0mA≦I_{OUT}≦100mA	-	14	80	-	14	80	mV
				1.0mA≦I_{OUT}≦40mA	-	6.5	40	-	6.5	40	
Output Voltage	V_{OUT}	1	9.8V≦V_{IN}≦23V, 1.0mA≦I_{OUT}≦40mA		6.9	-	8.1	7.125	-	7.875	V
			V_{IN}=13V, 1.0mA≦I_{OUT}≦70mA		6.9	-	8.1	7.125	-	7.875	
Quiescent Current	I_B	1	T_j=25°C		-	3.1	6.5	-	3.1	6.5	mA
			T_j=125°C		-	-	6.0	-	-	6.0	
Quiescent Current Change	ΔI_B	1	10.5V≦V_{IN}≦23V		-	-	1.5	-	-	1.5	mA
			1.0mA≦I_{OUT}≦40mA		-	-	0.2	-	-	0.1	
Output Noise Voltage	V_{NO}	1	Ta=25°C, 10Hz≦f≦100kHz		-	60	-	-	60	-	μV
Long Term Stability	$\Delta V_{OUT}/\Delta t$	1			-	19	-	-	19	-	mV/1.0 KHrs
Ripple Rejection	RR	2	f=120Hz, 11V≦V_{IN}≦21V, T_j=25°C		36	45	-	37	45	-	dB
Dropout Voltage	$\lvert V_{IN}-V_{OUT}\rvert$	1	T_j=25°C		-	1.7	-	-	1.7	-	V
Average Temperature Coefficient of Output Voltage	TC_{VO}	1	I_{OUT}=5mA		-	-0.75	-	-	-0.75	-	mV/°C

TA78L008P/AP ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, V_{IN}=14V, I_{OUT}=40mA, C_{IN}=0.33μF, C_{OUT}=0.1μF, $0^{o}C < T_j < 125^{o}C$)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION		TA78L008P			TA78L008AP			UNIT
					MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Output Voltage	V_{OUT}	1	$T_j=25^{o}C$		7.48	8.0	8.52	7.7	8.0	8.3	V
Input Regulation	Reg.line	1	$T_j=25^{o}C$	$10.5V \leqq V_{IN} \leqq 23V$	-	20	200	-	20	175	mV
				$11V \leqq V_{IN} \leqq 23V$	-	12	150	-	12	125	
Load Regulation	Reg.load	1	$T_j=25^{o}C$	$1.0mA \leqq I_{OUT} \leqq 100mA$	-	15	80	-	15	80	mV
				$1.0mA \leqq I_{OUT} \leqq 40mA$	-	7.0	40	-	7.0	40	
Output Voltage	V_{OUT}	1	$10.5V \leqq V_{IN} \leqq 23V$, $1.0mA \leqq I_{OUT} \leqq 40mA$		7.36	-	8.64	7.6	-	8.4	V
			V_{IN}=14V, $1.0mA \leqq I_{OUT} \leqq 70mA$		7.36	-	8.64	7.6	-	8.4	
Quiescent Current	I_B	1	$T_j=25^{o}C$		-	3.1	6.5	-	3.1	6.5	mA
			$T_j=125^{o}C$		-	-	6.0	-	-	6.0	
Quiescent Current Change	ΔI_B	1	$11V \leqq V_{IN} \leqq 23V$		-	-	1.5	-	-	1.5	mA
			$1.0mA \leqq I_{OUT} \leqq 40mA$		-	-	0.2	-	-	0.1	
Output Noise Voltage	V_{NO}	1	$Ta=25^{o}C$, $10Hz \leqq f \leqq 100kHz$		-	60	-	-	60	-	μV
Long Term Stability	$\Delta V_{OUT}/\Delta t$	1			-	20	-	-	20	-	mV/1.0 KHrs
Ripple Rejection	RR	2	f=120Hz, $12V \leqq V_{IN} \leqq 23V$, $T_j=25^{o}C$		36	45	-	37	45	-	dB
Dropout Voltage	$\|V_{IN}-V_{OUT}\|$	1	$T_j=25^{o}C$		-	1.7	-	-	1.7	-	V
Average Temperature Coefficient of Output Voltage	TC_{VO}	1	I_{OUT}=5mA		-	-0.8	-	-	-0.8	-	$mV/^{o}C$

TA78L005P/AP ~TA78L024P/AP

TA78L009P/AP ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, V_{IN}=15V, I_{OUT}=40mA, C_{IN}=0.33μF, C_{OUT}=0.1μF, $0^{\circ}C < T_j < 125^{\circ}C$)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION		TA78L009P MIN.	TA78L009P TYP.	TA78L009P MAX.	TA78L009AP MIN.	TA78L009AP TYP.	TA78L009AP MAX.	UNIT
Output Voltage	V_{OUT}	1	$T_j=25^{\circ}C$		8.42	9.0	9.58	8.64	9.0	9.36	V
Input Regulation	Reg.line	1	$T_j=25^{\circ}C$	$11.4V \leq V_{IN} \leq 24V$	-	80	230	-	80	200	mV
				$12V \leq V_{IN} \leq 24V$	-	20	160	-	20	160	
Load Regulation	Reg.load	1	$T_j=25^{\circ}C$	$1.0mA \leq I_{OUT} \leq 100mA$	-	17	90	-	17	90	mV
				$1.0mA \leq I_{OUT} \leq 40mA$	-	8.0	45	-	8.0	45	
Output Voltage	V_{OUT}	1	$11.4V \leq V_{IN} \leq 24V$ $1.0mA \leq I_{OUT} \leq 40mA$		8.28	-	9.72	8.55	-	9.45	V
			V_{IN}=15V, $1.0mA \leq I_{OUT} \leq 70mA$		8.28	-	9.72	8.55	-	9.45	
Quiescent Current	I_B	1	$T_j=25^{\circ}C$		-	3.2	6.5	-	3.2	6.5	mA
			$T_j=125^{\circ}C$		-	-	6.0	-	-	6.0	
Quiescent Current Change	ΔI_B	1	$11.5V \leq V_{IN} \leq 26V$		-	-	1.5	-	-	1.5	mA
			$1.0mA \leq I_{OUT} \leq 40mA$		-	-	0.2	-	-	0.1	
Output Noise Voltage	V_{NO}	1	$Ta=25^{\circ}C$, $10Hz \leq f \leq 100kHz$		-	65	-	-	65	-	μV
Long Term Stability	$\Delta V_{OUT}/\Delta t$	1			-	21	-	-	21	-	mV/1.0 KHrs
Ripple Rejection	RR	2	f=120Hz, $12V \leq V_{IN} \leq 24V$, $T_j=25^{\circ}C$		36	44	-	36	44	-	dB
Dropout Voltage	$\lvert V_{IN}-V_{OUT} \rvert$	1	$T_j=25^{\circ}C$		-	1.7	-	-	1.7	-	V
Average Temperature Coefficient of Output Voltage	TC_{VO}	1	I_{OUT}=5mA		-	+0.85	-	-	+0.85	-	mV/°C

TA78L010P/AP ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, V_{IN}=16V, I_{OUT}=40mA, C_{IN}=0.33μF, C_{OUT}=0.1μF, $0^{\circ}C \leq T_j \leq 125^{\circ}C$)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	TA78L010P MIN.	TA78L010P TYP.	TA78L010P MAX.	TA78L010AP MIN.	TA78L010AP TYP.	TA78L010AP MAX.	UNIT
Output Voltage	V_{OUT}	1	$T_j=25^{\circ}C$	9.35	10	10.65	9.6	10	10.4	V
Input Regulation	Reg. Line	1	$T_j=25^{\circ}C$, $12.5V \leq V_{IN} \leq 25V$	-	80	230	-	80	230	mV
			$T_j=25^{\circ}C$, $13V \leq V_{IN} \leq 25V$	-	30	170	-	30	170	mV
Load Regulation	Reg. load	1	$T_j=25^{\circ}C$, $1.0mA \leq I_{OUT} \leq 100mA$	-	18	90	-	18	90	mV
			$T_j=25^{\circ}C$, $1.0mA \leq I_{OUT} \leq 40mA$	-	8.5	45	-	8.5	45	mV
Output Voltage	V_{OUT}	1	$12.5V \leq V_{IN} \leq 25V$, $1.0mA \leq I_{OUT} \leq 40mA$	9.2	-	10.8	9.5	-	10.5	V
			V_{IN}=16V, $1.0mA \leq I_{OUT} \leq 70mA$	9.2	-	1.08	9.5	-	1.05	V
Quiescent Current	I_B	1	$T_j=25^{\circ}C$	-	3.2	6.5	-	3.2	6.5	mA
			$T_j=125^{\circ}C$	-	-	6.0	-	-	6.0	mA
Quiescent Current Change	ΔI_B	1	$13V \leq V_{IN} \leq 25V$	-	-	1.5	-	-	1.5	mA
			$1.0mA \leq I_{OUT} \leq 40mA$	-	-	0.2	-	-	0.1	mA
Output Noise Voltage	V_{NO}	1	$Ta=25^{\circ}C$, $10Hz \leq f \leq 100kHz$	-	70	-	-	70	-	μV
Long Term Stability	$\Delta V_{OUT}/\Delta t$	1		-	22	-	-	22	-	mV/1.0 KHrs
Ripple Rejection	RR	2	f=120Hz, $13V \leq V_{IN} \leq 24V$, $T_j=25^{\circ}C$	36	43	-	36	43	-	dB
Dropout Voltage	$\lvert V_{IN}-V_{OUT} \rvert$	1	$T_j=25^{\circ}C$	-	1.7	-	-	1.7	-	V
Average Temperature Coefficient of Output Voltage	TC_{VO}	1	I_{OUT}=5mA	-	-0.9	-	-	-0.9	-	mV/°C

TA78L005P/AP ~TA78L024P/AP

TA78L012P/AP ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, V_{IN}=19V, I_{OUT}=40mA, C_{IN}=0.33μF, C_{OUT}=0.1μF, $0^\circ C < T_j < 125^\circ C$)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION		TA78L012P MIN.	TA78L012P TYP.	TA78L012P MAX.	TA78L012AP MIN.	TA78L012AP TYP.	TA78L012AP MAX.	UNIT
Output Voltage	V_{OUT}	1	$T_j=25^\circ C$		11.22	12	12.78	11.5	12	12.5	V
Input Regulation	Reg.line	1	$T_j=25^\circ C$	$14.5V \leqq V_{IN} \leqq 27V$	-	120	250	-	120	250	mV
				$16V \leqq V_{IN} \leqq 27V$	-	100	200	-	100	200	
Load Regulation	Reg.load	1	$T_j=25^\circ C$	$1.0mA \leqq I_{OUT} \leqq 100mA$	-	20	100	-	20	100	mV
				$1.0mA \leqq I_{OUT} \leqq 40mA$	-	10	50	-	10	50	
Output Voltage	V_{OUT}	1	$14.5V \leqq V_{IN} \leqq 27V$, $1.0mA \leqq I_{OUT} \leqq 40mA$		11.04	-	12.96	11.4	-	12.6	V
			V_{IN}=19V, $1.0mA \leqq I_{OUT} \leqq 70mA$		11.04	-	12.96	11.4	-	12.6	
Quiescent Current	I_B	1	$T_j=25^\circ C$		-	3.2	6.5	-	3.2	6.5	mA
			$T_j=125^\circ C$		-	-	6.0	-	-	6.0	
Quiescent Current Change	ΔI_B	1	$16V \leqq V_{IN} \leqq 27V$		-	-	1.5	-	-	1.5	mA
			$1.0mA \leqq I_{OUT} \leqq 40mA$		-	-	0.2	-	-	0.1	
Output Noise Voltage	V_{NO}	1	$Ta=25^\circ C$, $10Hz \leqq f \leqq 100kHz$		-	80	-	-	80	-	μV
Long Term Stability	$\Delta V_{OUT}/\Delta t$	1			-	24	-	-	24	-	mV/1.0 KHrs
Ripple Rejection	RR	2	f=120Hz, $15V \leqq V_{IN} \leqq 25V$, $T_j=25^\circ C$		36	41	-	36	41	-	dB
Dropout Voltage	$\lvert V_{IN}-V_{OUT} \rvert$	1	$T_j=25^\circ C$		-	1.7	-	-	1.7	-	V
Average Temperature Coefficient of Output Voltage	TC_{VO}	1	I_{OUT}=5mA		-	-1.0	-	-	-1.0	-	mV/°C

TA78L132P/AP ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, V_{IN}=21V, I_{OUT}=40mA, C_{IN}=0.33μF, C_{OUT}=0.1μF, $0^{\circ}C < T_j < 125^{\circ}C$)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION		TA78L132P MIN.	TA78L132P TYP.	TA78L132P MAX.	TA78L132AP MIN.	TA78L132AP TYP.	TA78L132AP MAX.	UNIT
Output Voltage	V_{OUT}	1	$T_j=25^{\circ}C$		12.34	13.2	14.06	12.67	13.2	13.73	V
Input Regulation	Reg.line	1	$T_j=25^{\circ}C$	$16V \leq V_{IN} \leq 28V$	-	125	270	-	125	270	mV
				$17V \leq V_{IN} \leq 28V$	-	105	225	-	105	225	
Load Regulation	Reg.load	1	$T_j=25^{\circ}C$	$1.0mA \leq I_{OUT} \leq 100mA$	-	22	120	-	22	120	mV
				$1.0mA \leq I_{OUT} \leq 40mA$	-	11	60	-	11	60	
Output Voltage	V_{OUT}	1	$16V \leq V_{IN} \leq 28V$, $1.0mA \leq I_{OUT} \leq 40mA$		12.14	-	14.26	12.54	-	13.86	V
			V_{IN}=21V, $1.0mA \leq I_{OUT} \leq 70mA$		12.14	-	14.26	12.54	-	13.86	
Quiescent Current	I_B	1	$T_j=25^{\circ}C$		-	3.2	6.5	-	3.2	6.5	mA
			$T_j=125^{\circ}C$		-	3.2	6.0	-	3.2	6.0	
Quiescent Current Change	ΔI_B	1	$17V \leq V_{IN} \leq 28V$		-	-	1.5	-	-	1.5	mA
			$1.0mA \leq I_{OUT} \leq 40mA$		-	-	0.2	-	-	0.1	
Output Noise Voltage	V_{NO}	1	$Ta=25^{\circ}C$, $10Hz \leq f \leq 100kHz$		-	90	-	-	90	-	μV
Long Term Stability	$\Delta V_{OUT}/\Delta t$	1			-	28	-	-	28	-	mV/1.0 KHrs
Ripple Rejection	RR	2	f=100Hz, $17V \leq V_{IN} \leq 27V$, $T_j=25^{\circ}C$		34	41	-	34	41	-	dB
Dropout Voltage	$\lvert V_{IN}-V_{OUT} \rvert$	1	$T_j=25^{\circ}C$		-	1.7	-	-	1.7	-	V
Average Temperature Coefficient of Output Voltage	TC_{VO}	1	I_{OUT}=5mA		-	-1.2	-	-	-1.2	-	mV/°C

TA78L005P/AP ~TA78L024P/AP

TA78L015P/AP ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, V_{IN}=23V, I_{OUT}=40mA, C_{IN}=0.33μF, C_{OUT}=0.1μF, $0^{\circ}C < T_j < 125^{\circ}C$)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION		TA78L015P MIN.	TA78L015P TYP.	TA78L015P MAX.	TA78L015AP MIN.	TA78L015AP TYP.	TA78L015AP MAX.	UNIT
Output Voltage	V_{OUT}	1	$T_j=25^{\circ}C$		14.03	15	15.97	14.4	15	15.6	V
Input Regulation	Reg.line	1	$T_j=25^{\circ}C$	$17.5V \leqq V_{IN} \leqq 30V$	-	130	300	-	130	300	mV
				$20V \leqq V_{IN} \leqq 30V$	-	110	250	-	110	250	
Load Regulation	Reg.load	1	$T_j=25^{\circ}C$	$1.0mA \leqq I_{OUT} \leqq 100mA$	-	25	150	-	25	150	mV
				$1.0mA \leqq I_{OUT} \leqq 40mA$	-	12	75	-	12	75	
Output Voltage	V_{OUT}	1	$17.5V \leqq V_{IN} \leqq 30V$, $1.0mA \leqq I_{OUT} \leqq 40mA$		13.8	-	16.2	14.25	-	15.75	V
			V_{IN}=23V, $1.0mA \leqq I_{OUT} \leqq 70mA$		13.8	-	16.2	14.25	-	15.75	
Quiescent Current	I_B	1	$T_j=25^{\circ}C$		-	3.3	6.5	-	3.3	6.5	mA
			$T_j=125^{\circ}C$		-	-	6.0	-	-	6.0	
Quiescent Current Change	ΔI_B	1	$20V \leqq V_{IN} \leqq 30V$		-	-	1.5	-	-	1.5	mA
			$1.0mA \leqq I_{OUT} \leqq 40mA$		-	-	0.2	-	-	0.1	
Output Noise Voltage	V_{NO}	1	$Ta=25^{\circ}C$, $10Hz \leqq f \leqq 100kHz$		-	90	-	-	90	-	μV
Long Term Stability	$\Delta V_{OUT}/\Delta t$	1			-	30	-	-	30	-	mV/1.0 KHrs
Ripple Rejection	RR	2	f=120Hz, $18.5V \leqq V_{IN} \leqq 28.5V$, $T_j=25^{\circ}C$		33	40	-	34	40	-	dB
Dropout Voltage	$\lvert V_{IN}-V_{OUT} \rvert$	1	$T_j=25^{\circ}C$		-	1.7	-	-	1.7	-	V
Average Temperature Coefficient of Output Voltage	TC_{VO}	1	I_{OUT}=5mA		-	-1.3	-	-	-1.3	-	mV/°C

TA78L018P/AP ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, V_{IN}=27V, I_{OUT}=40mA, C_{IN}=0.33μF, C_{OUT}=0.1μF, $0^{\circ}C < T_j < 125^{\circ}C$)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION		TA78L018P			TA78L018AP			UNIT
					MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Output Voltage	V_{OUT}	1	$T_j=25^{\circ}C$		16.83	18	19.17	17.3	18	18.7	V
Input Regulation	Reg.line	1	$T_j=25^{\circ}C$	$21.4V \leqq V_{IN} \leqq 33V$	-	32	325	-	32	325	mV
				$22V \leqq V_{IN} \leqq 33V$	-	27	275	-	27	275	
Load Regulation	Reg.load	1	$T_j=25^{\circ}C$	$1.0mA \leqq I_{OUT} \leqq 100mA$	-	30	170	-	30	170	mV
				$1.0mA \leqq I_{OUT} \leqq 40mA$	-	15	75	-	15	75	
Output Voltage	V_{OUT}	1	$21.4V \leqq V_{IN} \leqq 33V$, $1.0mA \leqq I_{OUT} \leqq 40mA$		16.56	-	19.44	17.1	-	18.9	V
			$V_{IN}=27V$, $1.0mA \leqq I_{OUT} \leqq 70mA$		16.56	-	19.44	17.1	-	18.9	
Quiescent Current	I_B	1	$T_j=25^{\circ}C$		-	3.3	6.5	-	3.3	6.5	mA
			$T_j=125^{\circ}C$		-	-	6.0	-	-	6.0	
Quiescent Current Change	ΔI_B	1	$22V \leqq V_{IN} \leqq 33V$		-	-	1.5	-	-	1.5	mA
			$1.0mA \leqq I_{OUT} \leqq 40mA$		-	-	0.2	-	-	0.1	
Output Noise Voltage	V_{NO}	1	$Ta=25^{\circ}C$, $10Hz \leqq f \leqq 100kHz$		-	150	-	-	150	-	μV
Long Term Stability	$\Delta V_{OUT}/\Delta t$	1			-	45	-	-	45	-	mV/1.0 KHrs
Ripple Rejection	RR	2	f=120Hz, $23V \leqq V_{IN} \leqq 33V$, $T_j=25^{\circ}C$		32	38	-	32	38	-	dB
Dropout Voltage	$\|V_{IN}-V_{OUT}\|$	1	$T_j=25^{\circ}C$		-	1.7	-	-	1.7	-	V
Average Temperature Coefficient of Output Voltage	TC_{VO}	1	$I_{OUT}=5mA$		-	-1.5	-	-	-1.5	-	mV/°C

TA78L005P/AP ~TA78L024P/AP

TA78L020P/AP ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, V_{IN}=29V, I_{OUT}=40mA, C_{IN}=0.33μF, C_{OUT}=0.1μF, 0°C<T_j<125°C)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION		TA78L020P MIN.	TA78L020P TYP.	TA78L020P MAX.	TA78L020AP MIN.	TA78L020AP TYP.	TA78L020AP MAX.	UNIT
Output Voltage	V_{OUT}	1	T_j=25°C		18.7	20	21.3	19.2	20	20.8	V
Input Regulation	Reg.line	1	T_j=25°C	23.5V≦V_{IN}≦35V	-	33	330	-	33	330	mV
				24V≦V_{IN}≦35V	-	28	285	-	28	285	
Load Regulation	Reg.load	1	T_j=25°C	1.0mA≦I_{OUT}≦100mA	-	33	180	-	33	180	mV
				1.0mA≦I_{OUT}≦40mA	-	17	90	-	17	90	
Output Voltage	V_{OUT}	1	23.5V≦V_{IN}≦35V, 1.0mA≦I_{OUT}≦40mA		18.4	-	21.6	19.0	-	21.0	V
			V_{IN}=29V, 1.0mA≦I_{OUT}≦70mA		18.4	-	21.6	19.0	-	21.0	
Quiescent Current	I_B	1	T_j=25°C		-	3.3	6.5	-	3.3	6.5	mA
			T_j=125°C		-	-	6.0	-	-	6.0	
Quiescent Current Change	ΔI_B	1	24V≦V_{IN}≦35V		-	-	1.5	-	-	1.5	mA
			1.0mA≦I_{OUT}≦40mA		-	-	0.2	-	-	0.1	
Output Noise Voltage	V_{NO}	1	Ta=25°C, 10Hz≦f≦100kHz		-	170	-	-	170	-	μV
Long Term Stability	$\Delta V_{OUT}/\Delta t$	1			-	49	-	-	49	-	mV/1.0 KHrs
Ripple Rejection	RR	2	f=120Hz, 25V≦V_{IN}≦35V, T_j=25°C		31	37	-	31	37	-	dB
Dropout Voltage	$\lvert V_{IN}-V_{OUT}\rvert$	1	T_j=25°C		-	1.7	-	-	1.7	-	V
Average Temperature Coefficient of Output Voltage	TC_{VO}	1	I_{OUT}=5mA		-	-1.7	-	-	-1.7	-	mV/°C

TA78L024P/AP ELECTRICAL CHARACTERISTICS

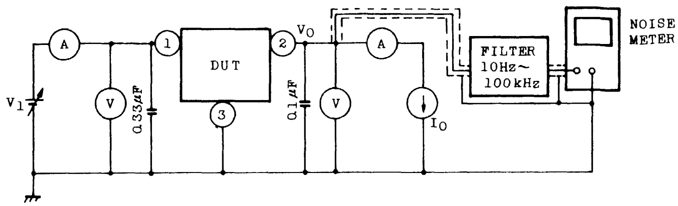
(Unless otherwise specified, V_{IN}=33V, I_{OUT}=40mA, C_{IN}=0.33μF, C_{OUT}=0.1μF, $0^\circ C < T_j < 125^\circ C$)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION		TA78L024P			TA78L024AP			UNIT
					MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Output Voltage	V_{OUT}	1	$T_j=25^\circ C$		22.44	24	25.56	23	24	25	V
Input Regulation	Reg.line	1	$T_j=25^\circ C$	$27.5V \leq V_{IN} \leq 38V$	-	35	350	-	35	350	mV
				$28V \leq V_{IN} \leq 38V$	-	30	300	-	30	300	
Load Regulation	Reg.load	1	$T_j=25^\circ C$	$1.0mA \leq I_{OUT} \leq 100mA$	-	40	200	-	40	200	mV
				$1.0mA \leq I_{OUT} \leq 40mA$	-	20	100	-	20	100	
Output Voltage	V_{OUT}	1	$27.5V \leq V_{IN} \leq 38V$, $1.0mA \leq I_{OUT} \leq 40mA$		22.08	-	25.92	22.8	-	25.2	V
			V_{IN}=33V, $1.0mA \leq I_{OUT} \leq 70mA$		22.08	-	25.92	22.8	-	25.2	
Quiescent Current	I_B	1	$T_j=25^\circ C$		-	3.5	6.5	-	3.5	6.5	mA
			$T_j=125^\circ C$		-	-	6.0	-	-	6.0	
Quiescent Current Change	ΔI_B	1	$28V \leq V_{IN} \leq 38V$		-	-	1.5	-	-	1.5	mA
			$1.0mA \leq I_{OUT} \leq 40mA$		-	-	0.2	-	-	0.1	
Output Noise Voltage	V_{NO}	1	$Ta=25^\circ C$, $10Hz \leq f \leq 100kHz$		-	200	-	-	200	-	μV
Long Term Stability	$\Delta V_{OUT} / \Delta t$	1			-	56	-	-	56	-	mV / 1.0 KHrs
Ripple Rejection	RR	2	f=120Hz, $29V \leq V_{IN} \leq 39V$, $T_j=25^\circ C$		30	35	-	31	35	-	dB
Dropout Voltage	$\lvert V_{IN}-V_{OUT} \rvert$	1	$T_j=25^\circ C$		-	1.7	-	-	1.7	-	V
Average Temperature Coefficient of Output Voltage	TC_{VO}	1	I_{OUT}=5mA		-	-2.0	-	-	-2.0	-	mV/°C

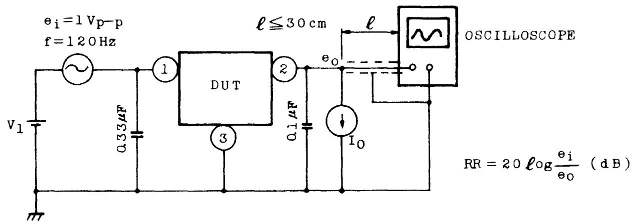
TA78L005P/AP
~TA78L024P/AP

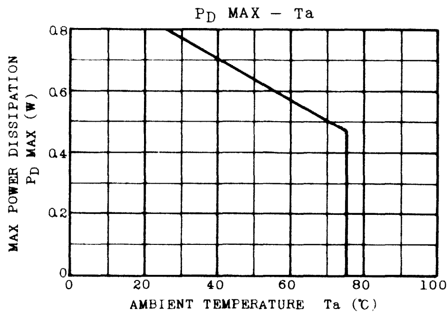
TEST CIRCUIT

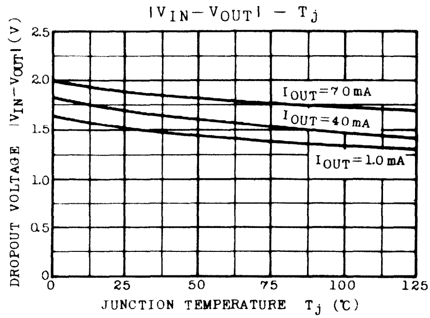
1. V_{OUT}, Reg.line, Reg.load, V_{OUT}, I_B, ΔI_B, V_{NO}, $\Delta V_{OUT}/\Delta t$, $|V_{IN}-V_{OUT}|$, TC_{VO}

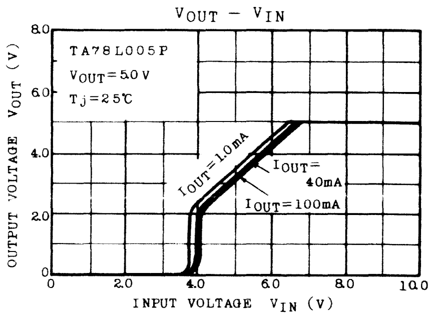


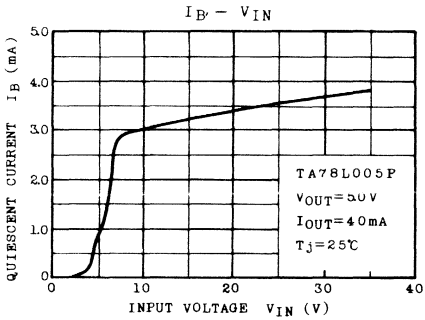
2. RR

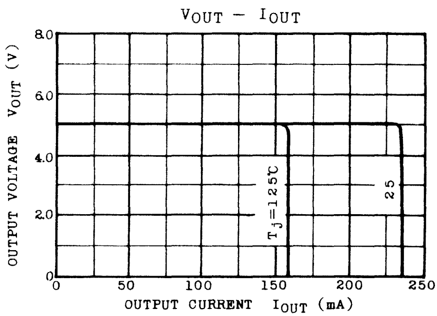



P_D MAX − Ta
MAX POWER DISSIPATION P_D MAX (W)
AMBIENT TEMPERATURE Ta (℃)


$|V_{IN}-V_{OUT}|$ − T_j
DROPOUT VOLTAGE $|V_{IN}-V_{OUT}|$ (V)
I_{OUT}=70 mA
I_{OUT}=40 mA
I_{OUT}=1.0 mA
JUNCTION TEMPERATURE T_j (℃)


V_{OUT} − V_{IN}
TA78L005P
V_{OUT}=5.0 V
T_j=25℃
I_{OUT}=1.0 mA
I_{OUT}= 40mA
I_{OUT}=100mA
OUTPUT VOLTAGE V_{OUT} (V)
INPUT VOLTAGE V_{IN} (V)

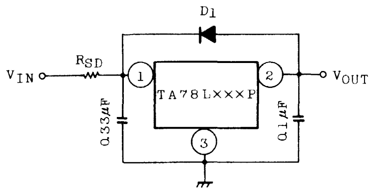

$I_{B'}$ − V_{IN}
TA78L005P
V_{OUT}=5.0 V
I_{OUT}=40 mA
T_j=25℃
QUIESCENT CURRENT I_B (mA)
INPUT VOLTAGE V_{IN} (V)


V_{OUT} − I_{OUT}
T_j=125℃
25
OUTPUT VOLTAGE V_{OUT} (V)
OUTPUT CURRENT I_{OUT} (mA)

TA78L005P/AP ~TA78L024P/AP

APPLICATION CIRCUIT

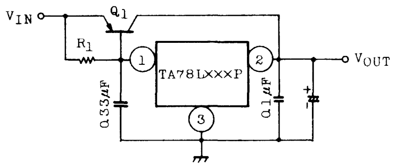
(1) STANDARD APPLICATION



D_1 : Protection Diode
High speed diode D_1 should be connected as shown in the figure if the condition $V_{IN} < V_{OUT}$ might occur by surge voltage or power supply ON/OFF.

R_{SD} : Power Limiting Resistor
For large V_{IN}, resistor R_{SD} is needed to limit IC power dissipation.

(2) A. CURRENT BOOST VOLTAGE REGULATOR



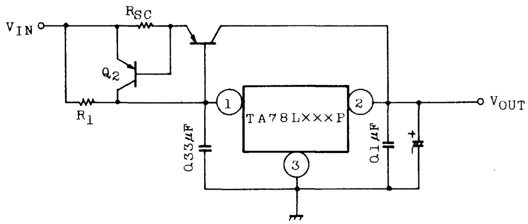
Heat sink is needed for Q_1

$$R_1 \leq \frac{V_{BE1}}{I_B\ MAX}$$

where, V_{BE1} : V_{BE} of external transistor Q_1

I_B MAX : Quiescent current of IC

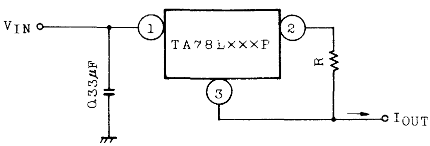
B. SHORT-CIRCUIT PROTECTION



$$R_{SC} = \frac{V_{BE2}}{I_{SC}}$$

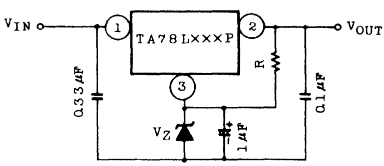
where, I_{SC} : Short-Circuit current

(3) CURRENT REGULATOR



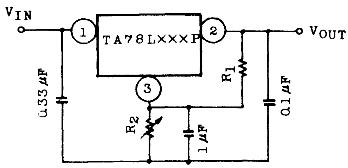
$$I_{OUT} = \frac{V_{OUT}}{R} + I_B$$

(4) VOLTAGE BOOST REGULATOR



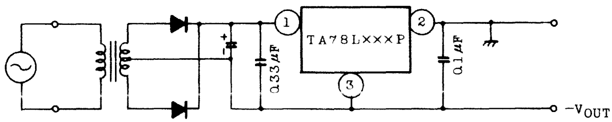
$V_{OUT}=V_Z+V_{OUT}$(of IC)

A little of current in resistor R is needed.

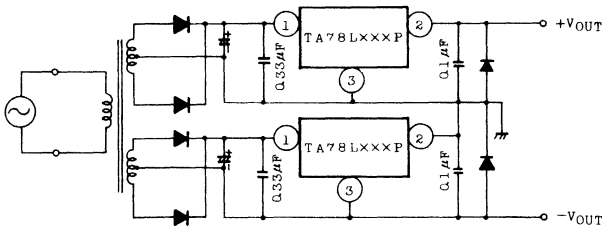


$V_{OUT}=R_2(I_B \cdot \frac{V_{OUT}\text{(of IC)}}{R_1}) + V_{OUT}\text{(of IC)}$

(5) NEGATIVE REGULATOR



(6) POSITIVE AND NEGATIVE REGULATOR



TA78L005P/AP ~TA78L024P/AP

PRECAUTIONS FOR USE

When such a high voltage as exceeds 10V beyond the fixed output voltage (TYP Value) of IC is applied to the output terminal of IC, the IC may be destroyed. In such a case, it is advised to prevent an excessive voltage from being applied to the IC by connecting a zener diode between the output terminal and the GND. Especially, in the current boost circuit as shown in Example (2) of Application Circuits, an input voltage may be suddenly applied to the output terminal of IC in the form of steps, and that in case of light load, an excessive voltage may be transiently applied to the output terminal of IC: So that great care should be taken to this matter. In this case, in addition to the above, it may become necessary to consider such a countermeasure as the output capacitor in use is replaced with a capacitor of larger capacitance, or as R_1 (a resistor for IC bias current or bypass is replaced with a resistor of smaller resistance according to circumstances, or as the input voltage is gradually raised.

BIPOLAR LINEAR INTEGRATED CIRCUIT
SILICON MONOLITHIC

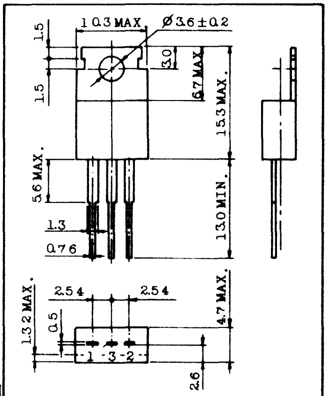
TA79005P～TA79024P

1A THREE TERMINAL NEGATIVE VOLTAGE REGULATORS

-5V, -6V, -8V, -9V, -10V, -12V, -15V, -18V, -20V, -24V

- Suitable for C-MOS, TTL, and the other Digital IC Power Supply
- Internal Thermal Overload Protecting
- Internal Short Circuit Current Limiting
- Output Current in Excess of 1.0A
- Package in the Plastic Case TO-220AB

Unit in mm



1. GND
2. OUTPUT
3. INPUT (CASE)

JEDEC	TO-220AB
EIAJ	SC-46
TOSHIBA	5-10A

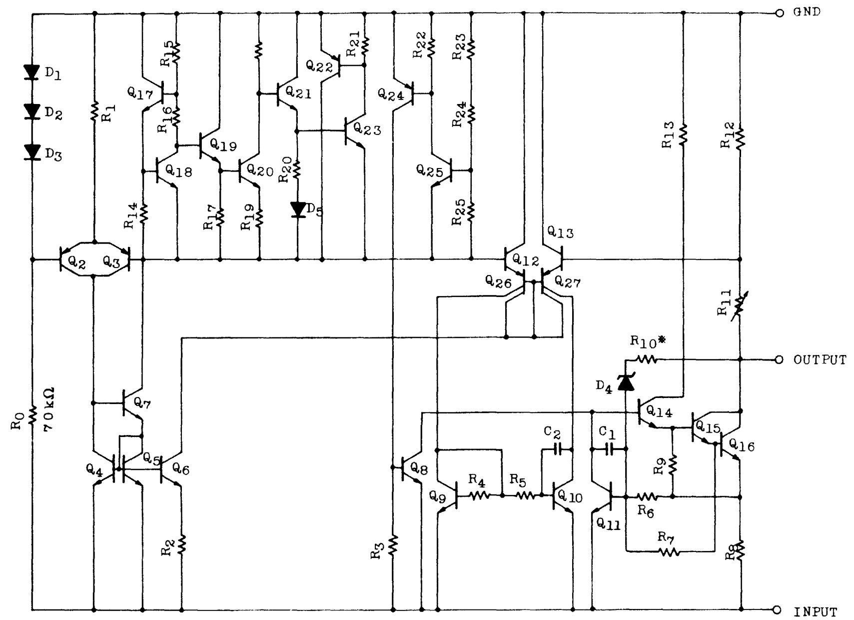
Mounting Kit No. AC75

MAXIMUM RATINGS (Ta=25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Input Voltage	TA79005P	V_{IN}	-35	V
	TA79006P			
	TA79008P			
	TA79009P			
	TA79010P			
	TA79012P			
	TA79015P			
Input Voltage	TA79018P	V_{IN}	-40	V
	TA79020P			
	TA79024P			
Power Dissipation (Tc=25°C)		P_D	20.8	W
Operating Temperature		Topr	-30～75	°C
Storage Temperature		Tstg	-55～125	°C

TA79005P ~ TA79024P

EQUIVALENT CIRCUIT



TA79005P ~ TA79024P

TA79005P

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{IN}=-10V, I_{OUT}=500mA, 0°C<Tj ≤125°C
C_{IN}=1.0μF, C_{OUT}=1.0μF

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Output Voltage		V_{OUT}	1	Tj=25°C		-4.8	-5.0	-5.2	V
Input Regulation		Reg·Line	1	Tj=25°C	-25V ≦ V_{IN} ≦ -7V I_{OUT}=100mA	–	7.0	50	mV
					-25V ≦ V_{IN} ≦ -7V I_{OUT}=500mA	–	35	100	mV
Load Regulation		Reg·Load	1	Tj=25°C	5mA ≦ I_{OUT} ≦ 1.5A	–	11	100	mV
					250mA ≦ I_{OUT} ≦ 750mA	–	4.0	50	mV
Output Voltage		V_{OUT}	1	-20V ≦ V_{IN} ≦ -7V 5mA ≦ I_{OUT} ≦ 1.0A		-4.75	–	-5.25	V
Quiescent Current		I_B	1	Tj=25°C		–	4.3	8.0	mA
Quiescent Current Charge	Line	ΔI_{BO}	1	-25V ≦ V_{IN} ≦ -7V		–	–	1.3	mA
	Load	ΔI_{BI}	1	1.0A ≦ I_{OUT} ≦ 5mA		–	–	0.5	mA
Output Noise Voltage		V_{NO}	2	Ta=25°C, 10Hz ≦ f ≦ 100kHz		–	40	–	μV
Ripple Rejection		RR	3	f=120Hz, I_{OUT}=20mA		63	70	–	dB
Short Circuit Current Limit		I_{SC}	1	Tj=25°C		–	1.9	–	A
Average Temperature Coefficient Output Voltage		T_{CVO}	1	I_{OUT}=5.0mA		–	-0.3	–	mV/deg
Dropout Voltage		V_D	1	Ta=25°C		–	2.0	–	V

TA79005P～TA79024P

TA79006P

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{IN}=-11V, I_{OUT}=500mA, 0°C≦Tj≦125°C
C_{IN}=1.0μF, C_{OUT}=1.0μF

CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Output Voltage		V_{OUT}	1	Tj=25°C		-5.75	-6.0	-6.25	V
Input Regulation		Reg·Line	1	Tj=25°C	-25V≦V_{IN}≦-8V I_{OUT}=100mA	-	9.0	60	mV
					-25V≦V_{IN}≦-8V I_{OUT}=500mA	-	43	120	mV
Load Regulation		Reg·Load	1	Tj=25°C	5mA≦I_{OUT}≦1.5A	-	13	120	mV
					250mA≦I_{OUT}≦750mA	-	5.0	60	mV
Output Voltage		V_{OUT}	1	-21V≦V_{IN}≦-8V 5mA≦I_{OUT}≦1.0A		-5.7	-	-6.3	V
Quiescent Current		I_B	1	T_j=25°C		-	4.3	8.0	mA
Quiescent Current Charge	Line	ΔI_{BO}	1	-25V≦V_{IN}≦-8V		-	-	1.3	mA
	Load	ΔI_{BI}	1	1.0A≦I_{OUT}≦5mA		-	-	0.5	mA
Output Noise Voltage		V_{NO}	2	Ta=25°C, 10Hz≦f≦100kHz		-	45	-	μV
Ripple Rejection		RR	3	f=120Hz, I_{OUT}=20mA		58	65	-	dB
Short Circuit Current Limit		I_{SC}	1	Tj=25°C		-	1.9	-	A
Average Temperature Coefficient Output Voltage		T_{CVO}	1	I_{OUT}=5.0mA		-	-0.3	-	mV/deg
Dropout Voltage		V_D	1	Ta=25°C		-	2.0	-	V

TA79008P

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{IN}=14V, I_{OUT}=500mA, 0°C≦Tj≦125°C
C_{IN}=1.0μF, C_{OUT}=1.0μF

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Output Voltage		V_{OUT}	1	Tj=25°C		-7.7	-8.0	-8.3	V
Input Regulation		Reg·Line	1	Tj=25°C	-25V≦V_{IN}≦-10.5V I_{OUT}=100mA	-	11	80	mV
					-25V≦V_{IN}≦-10.5V I_{OUT}=500mA	-	47	160	mV
Load Regulation		Reg·Load	1	Tj=25°C	5mA≦I_{OUT}≦1.5A	-	26	160	mV
					250mA≦I_{OUT}≦750mA	-	9.0	80	mV
Output Voltage		V_{OUT}	1	-23V≦V_{IN}≦-10.5V 5mA≦I_{OUT}≦1.0A		-7.6	-	-8.4	V
Quiescent Current		I_B	1	Tj=25°C		-	4.3	8.0	mA
Quiescent Current Charge	Line	ΔI_{BO}	1	-25V≦V_{IN}≦-10.5V		-	-	1.0	mA
	Load	ΔI_{BI}	1	1.0A≦I_{OUT}≦5mA		-	-	0.5	mA
Output Noise Voltage		V_{NO}	2	Ta=25°C, 10Hz≦f≦100kHz		-	52	-	μV
Ripple Rejection		RR	3	f=120Hz, I_{OUT}=20mA		55	62	-	dB
Short Circuit Current Limit		I_{SC}	1	Tj=25°C		-	1.9	-	A
Average Temperature Coefficient Output Voltage		T_{CVO}	1	I_{OUT}=5.0mA		-	-0.4	-	mV/deg
Dropout Voltage		V_D	1	Ta=25°C		-	2.0	-	V

TA79005P～TA79024P

TA79009P

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{IN}=-15V, I_{OUT}=500mA, 0°C≦Tj≦125°C
C_{IN}=1.0μF, C_{OUT}=1.0μF

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Output Voltage		V_{OUT}	1	Tj=25°C		-8.7	-9.0	-9.3	V
Input Regulation		Reg·Line	1	Tj=25°C	-26V≦V_{IN}≦-11.5V I_{OUT}=100mA	-	11	82	mV
					-26V≦V_{IN}≦-11.5V I_{OUT}=500mA	-	48	162	mV
Load Regulation		Reg·Load	1	Tj=25°C	5mA≦I_{OUT}≦1.5A	-	33	162	mV
					250mA≦I_{OUT}≦750mA	-	11.0	82	mV
Output Voltage		V_{OUT}	1	-24V≦V_{IN}≦-11.5V 5mA≦I_{OUT}≦1.0A		-8.6	-	-9.4	V
Quiescent Current		I_B	1	Tj=25°C		-	4.3	8.0	mA
Quiescent Current Charge	Line	ΔI_{BO}	1	-26.5 V≦V_{IN}≦-13V		-	-	1.0	mA
	Load	ΔI_{BI}	1	1.0A≦I_{OUT}≦5mA		-	-	0.5	mA
Output Noise Voltage		V_{NO}	2	Ta=25°C, 10Hz≦f≦100kHz		-	60	-	μV
Ripple Rejection		RR	3	f=120Hz, I_{OUT}=20mA		54	61	-	dB
Short Circuit Current Limit		I_{SC}	1	Tj=25°C		-	1.9	-	A
Average Temperature Coefficient Output Voltage		T_{CVO}	1	I_{OUT}=5.0mA		-	-0.4	-	mV/deg
Dropout Voltage		V_D	1	Ta=25°C		-	2.0	-	V

TA79010P

ELECTRICAL CHARACTERISTICS

・Unless otherwise specified, V_{IN}=-16V, I_{OUT}=500mA, 0°C≦Tj≦125°C
C_{IN}=1.0μF, C_{OUT}=1.0μF

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Output Voltage		V_{OUT}	1	Tj=25°C		-9.6	-10	-10.4	V
Input Regulation		Reg・Line	1	Tj=25°C	-27V≦V_{IN}≦12.5V I_{OUT}=100mA	-	12	90	mV
					-27V≦V_{IN}≦-12.5V I_{OUT}=500mA	-	50	180	mV
Load Regulation		Reg・Load	1	Tj=25°C	5mA≦I_{OUT}≦1.5A	-	40	180	mV
					250mA≦I_{OUT}≦750mA	-	13.0	90	mV
Output Voltage		V_{OUT}	1	-25V≦V_{IN}≦-12.5V 5mA≦I_{OUT}≦1.0A		-9.5	-	-10.5	V
Quiescent Current		I_B	1	Tj=25°C		-	4.3	8.0	mA
Quiescent Current Charge	Line	ΔI_{BO}	1	-27.5V≦V_{IN}≦-14V		-	-	1.0	mA
	Load	ΔI_{BI}	1	1.0A≦I_{OUT}≦5mA		-	-	0.5	mA
Output Noise Voltage		V_{NO}	2	Ta=25°C, 10Hz≦f≦100kHz		-	65	-	μV
Ripple Rejection		RR	3	f=120Hz, I_{OUT}=20mA		54	61	-	dB
Short Circuit Current Limit		I_{SC}	1	Tj=25°C		-	1.9	-	A
Average Temperature Coefficient Output Voltage		T_{CVO}	1	I_{OUT}=5.0mA		-	-0.5	-	mV/deg
Dropout Voltage		V_D	1	Ta=25°C		-	2.0	-	V

TA79005P~TA79024P

TA79012P

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{IN}=−19V, I_{OUT}=500mA, 0°C≦Tj≦125°C
C_{IN}=1.0μF, C_{OUT}=1.0μF

CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Output Voltage		V_{OUT}	1	Tj=25°C		-11.5	-12	-12.5	V
Input Regulation		Reg·Line	1	Tj=25°C	−30V≦V_{IN}≦−14.5V I_{OUT}=100mA	-	13	120	mV
					−30V≦V_{IN}≦−14.5V I_{OUT}=500mA	-	55	240	mV
Load Regulation		Reg·Load	1	Tj=25°C	5mA≦I_{OUT}≦1.5A	-	46	240	mV
					250mA≦I_{OUT}≦750mA	-	17	120	mV
Output Voltage		V_{OUT}	1	−27V≦V_{IN}≦−14.5V 5mA≦I_{OUT}≦1.0A		-11.4	-	-1.26	V
Quiescent Current		I_B	1	Tj=25°C		-	4.3	8.0	mA
Quiescent Current Charge	Line	ΔI_{BO}	1	−30V≦V_{IN}≦−14.5V		-	-	1.0	mA
	Load	ΔI_{BI}	1	1.0A≦I_{OUT}≦5mA		-	-	0.5	mA
Output Noise Voltage		V_{NO}	2	Ta=25°C, 10Hz≦f≦100kHz		-	75	-	μV
Ripple Rejection		RR	3	f=120Hz, I_{OUT}=20mA		54	61	-	dB
Short Circuit Current Limit		I_{SC}	1	Tj=25°C		-	1.9	-	A
Average Temperature Coefficient Output Voltage		T_{CVO}	1	I_{OUT}=5.0mA		-	-0.6	-	mV/deg
Dropout Voltage		V_D	1	Ta=25°C		-	2.0	-	V

TA79015P

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{IN}=-23V, I_{OUT}=500mA, 0°C≦Tj≦125°C
C_{IN}=1.0μF, C_{OUT}=1.0μF

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Output Voltage		V_{OUT}	1	Tj=25°C		-14.4	-15	-15.6	V
Input Regulation		Reg・Line	1	Tj=25°C	-30V≦V_{IN}≦-17.5V I_{OUT}=100mA	-	14	150	mV
					-30V≦V_{IN}≦-17.5V I_{OUT}=500mA	-	57	300	mV
Load Regulation		Reg・Load	1	Tj=25°C	5mA≦I_{OUT}≦1.5A	-	68	300	mV
					250mA≦I_{OUT}≦750mA	-	25	150	mV
Output Voltage		V_{OUT}	1	-30V≦V_{IN}≦-17.5V 5mA≦I_{OUT}≦1.0A		-14.25	-	-15.75	V
Quiescent Current		I_B	1	Tj=25°C		-	4.3	8.0	mA
Quiescent Current Charge	Line	ΔI_{BO}	1	-30V≦V_{IN}≦-17.5V		-	-	1.0	mA
	Load	ΔI_{BI}	1	1.0A≦I_{OUT}≦5mA		-	-	0.5	mA
Output Noise Voltage		V_{NO}	2	Ta=25°C, 10Hz≦f≦100kHz		-	90	-	μV
Ripple Rejection		RR	3	f=120Hz, I_{OUT}=20mA		53	60	-	dB
Short Circuit Current Limit		I_{SC}	1	Tj=25°C		-	1.9	-	A
Average Temperature Coefficient Output Voltage		T_{CVO}	1	I_{OUT}=5.0mA		-	-0.7	-	mV/deg
Dropout Voltage		V_D	1	Ta=25°C		-	2.0	-	V

TA79005P～TA79024P

TA79018P

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{IN}=-27V, I_{OUT}=500mA, 0°C≦Tj≦125°C
C_{IN}=1.0μF, C_{OUT}=1.0μF

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Output Voltage		V_{OUT}	1	Tj=25°C		-17.3	-18	-18.7	V
Input Regulation		Reg・Line	1	Tj=25°C	-33V≦V_{IN}≦-21V I_{OUT}=100mA	-	25	180	mV
					-33V≦V_{IN}≦-21V I_{OUT}=500mA	-	80	360	mV
Load Regulation		Reg・Load	1	Tj=25°C	5mA≦I_{OUT}≦1.5A	-	110	360	mV
					250mA≦I_{OUT}≦750mA	-	55	180	mV
Output Voltage		V_{OUT}	1	-33V≦V_{IN}≦-21V 5mA≦I_{OUT}≦1.0A		-17.15	-	-18.85	V
Quiescent Current		I_B	1	Tj=25°C		-	4.3	8.0	mA
Quiescent Current Charge	Line	ΔI_{BO}	1	-33V≦V_{IN}≦-21V		-	-	1.0	mA
	Load	ΔI_{BI}	1	1.0A≦I_{OUT}≦5mA		-	-	0.5	mA
Output Noise Voltage		V_{NO}	2	Ta=25°C, 10Hz≦f≦100kHz		-	110	-	μV
Ripple Rejection		RR	3	f=120Hz, I_{OUT}=20mA		52	59	-	dB
Short Circuit Current Limit		I_{SC}	1	Tj=25°C		-	1.9	-	A
Average Temperature Coefficient Output Voltage		T_{CVO}	1	I_{OUT}=5.0mA		-	-0.8	-	mV/deg
Dropout Voltage		V_D	1	Ta=25°C		-	2.0	-	V

TA79005P～TA79024P

TA79020P

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{IN}=-30V, I_{OUT}=500mA, 0°C≦Tj≦125°C
C_{IN}=1.0μF, C_{OUT}=1.0μF

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Output Voltage		V_{OUT}	1	Tj=25°C		-19.2	-20	-20.8	V
Input Regulation		Reg·Line	1	Tj=25°C	-35V≦V_{IN}≦-24V I_{OUT}=100mA	-	28	180	mV
					-35V≦V_{IN}≦-24V I_{OUT}=500mA	-	104	360	mV
Load Regulation		Reg·Load	1	Tj=25°C	5mA≦I_{OUT}≦1.5A	-	130	360	mV
					250mA≦I_{OUT}≦750mA	-	70	180	mV
Output Voltage		V_{OUT}	1	-35V≦V_{IN}≦-24V 5mA≦I_{OUT}≦1.0A		-19.0	-	-22.0	V
Quiescent Current		I_B	1	Tj=25°C		-	4.3	8.0	mA
Quiescent Current Charge	Line	ΔI_{BO}	1	-36.5V≦V_{IN}≦-25V		-	-	1.0	mA
	Load	ΔI_{BI}	1	1.0A≦I_{OUT}≦5mA		-	-	0.5	mA
Output Noise Voltage		V_{NO}	2	Ta=25°C, 10Hz≦f≦100kHz		-	140	-	μV
Ripple Rejection		RR	3	f=120Hz, I_{OUT}=20mA		50	57	-	dB
Short Circuit Current Limit		I_{SC}	1	Tj=25°C		-	1.9	-	A
Average Temperature Coefficient Output Voltage		T_{CVO}	1	I_{OUT}=5.0mA		-	-0.9	-	mV/deg
Dropout Voltage		V_D	1	Ta=25°C		-	2.0	-	V

TA79005P ~ TA79024P

TA79024P

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{IN}=-33V, I_{OUT}=500mA, 0°C ≦ Tj ≦ 125°C
C_{IN}=1.0μF, C_{OUT}=1.0μF

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Output Voltage		V_{OUT}	1	Tj=25°C		-23	-24	-25	V
Input Regulation		Reg・Line	1	Tj=25°C	-38V ≦ V_{IN} ≦ -27V I_{OUT}=100mA	-	31	240	mV
					-38V ≦ V_{IN} ≦ -27V I_{OUT}=500mA	-	118	480	mV
Load Regulation		Reg・Load	1	Tj=25°C	5mA ≦ I_{OUT} ≦ 1.5A	-	150	480	mV
					250mA ≦ I_{OUT} ≦ 750mA	-	85	240	mV
Output Voltage		V_{OUT}	1	-38V ≦ V_{IN} ≦ -27V 5mA ≦ I_{OUT} ≦ 1.0A		-22.8	-	-25.2	V
Quiescent Current		I_B	1	Tj=25°C		-	4.3	8.0	mA
Quiescent Current Charge	Line	ΔI_{BO}	1	-38V ≦ V_{IN} ≦ -27V		-	-	1.0	mA
	Load	ΔI_{BI}	1	1.0A ≦ I_{OUT} ≦ 5mA		-	-	0.5	mA
Output Noise Voltage		V_{NO}	1	Ta=25°C, 10Hz ≦ f ≦ 100kHz		-	170	-	μV
Ripple Rejection		RR	1	f=120Hz, I_{OUT}=20mA		49	56	-	dB
Short Circuit Current Limit		I_{SC}	1	Tj=25°C		-	1.9	-	A
Average Temperature Coefficient Output Voltage		T_{CVO}	1	I_{OUT}=5.0mA		-	-1.0	-	mV/deg
Dropout Voltage		V_D	1	Ta=25°C		-	2.0	-	V

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